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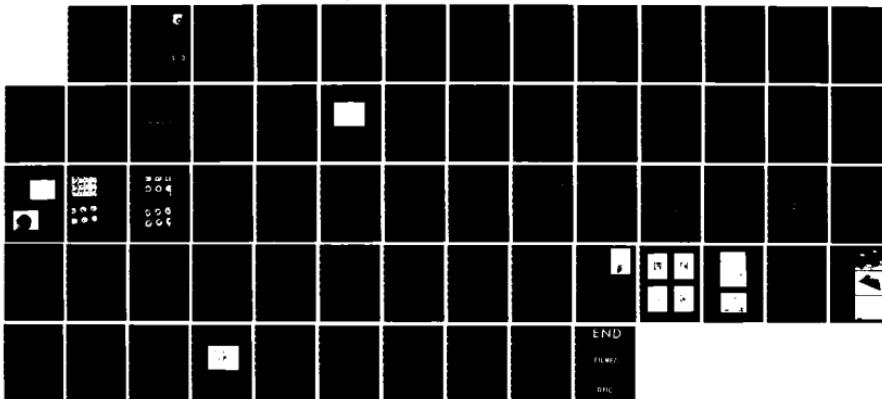
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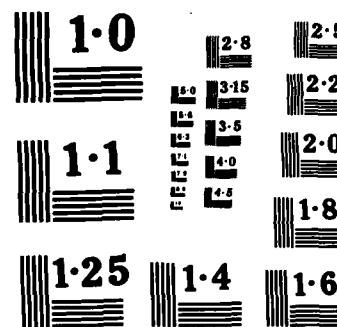
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MICROCOPY RESOLUTION TEST CHART

AD-A156 216

AFWAL-TR-84-3029

FLAT PANEL AIRCRAFT VIDEO LED DISPLAY  
TECHNOLOGY PROGRAM

Optotek Limited  
1283 Algoma Road  
Ottawa, Ontario  
Canada K1B 3W7



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Canada

December 1983

Final Report for Period September 1980 - July 1983

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This technical report has been reviewed and is approved for publication.

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eight level grey scale with a grey scale ratio of 2. In addition, array sections were fabricated confirming the achievement of sunlight visible performance for 128 lines-per-inch LED arrays.

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128 lines-per-inch

128

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## PREFACE

This document reports the results of research activities sponsored by USAF (FDL) in conjunction with the Canadian Department of Industry Trade and Commerce (DITC) and Optotek Limited.

Basic investigations were conducted into the fabrication and assembly of modular 1"x1" LED arrays of resolution 128 lines-per-inch. The LED material used was green-emitting gallium phosphide. Various LED configurations were investigated including stitch-bonded and flip-chip structures. A demonstration display system was built and delivered to the USAF/FDL; this consisted of a 1"x1" array plus associated decode/drive electronics interfaced to a 128x128 matrix solid-state TV camera. The electronics provided for the generation of video imagery on an eight level grey scale with a grey scale ratio of  $\sqrt{2}$ . In addition, sectional arrays were fabricated confirming the achievement of sunlight visible performance for 128 lines-per-inch LED arrays.

Under an Optotek/DITC funded continuation of the USAF/DITC contract, effort was applied to the fabrication of higher performance 1"x1" 128 lines-per-inch arrays. Insight was gained into limitations affecting the resolution achievable for abutable, sunlight visible LED video displays. It was concluded that the practical resolution limit is of the order of 100 lines-per-inch.

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## 1.0 INTRODUCTION

Work on the LED video display development program commenced in September, 1980. At that time the USAF/Canadian Commercial Corporation (CCC) contract had been signed. In February, 1981, the complementary Canadian Department of Industry, Trade & Commerce (DITC) contract was awarded to Optotek Limited, with provision for retroactivity to September 1980. The duration of the program was originally estimated at 13 months but program completion dates were later extended to 30 months to allow completion of supplementary work jointly funded by the company and DITC.

The technical task involved the design and fabrication of a 125 line-per-inch video resolution LED array in a 128x128-element abuttable-module configuration. This configuration facilitates the construction of a screen of any desired size. It was envisaged that ultimately decode drive electronics would be integrated behind the LED surface in a manner compatible with this size-expansion concept.

The scale and scope of the USAF/DITC program did not include provision for the fabrication of the integrated drive electronics; this miniaturization task would have involved the design and acquisition of custom LSI drive circuits. The design and construction of the high-resolution LED array was considered the technology limiting factor. The 1"x1" array was, however, to be delivered with demonstration electronics utilizing TV camera input and incorporating at least 4 grey-scale levels.

Under the USAF/CCC/DITC contract a 128x128 element LED test array was constructed and interfaced with a solid-state TV camera. The pixel defect level was less than 2%. Grey-scale was extended to 8 shades; this circuitry performed well. Overall performance would have benefited from use of a higher-frame rate camera of the type which have become available recently. The video array demonstration system was delivered to the USAF in July, 1983.

The material used for fabrication of the array was not compatible with sunlight visibility. Separately a 125 line-per-inch array section (18x32 elements) was constructed which did demonstrate significantly improved light-output performance of the order required for sunlight visibility. The supplementary Optotek/DITC contract addressed the construction of a 1"x1" array using higher performance material. This supplementary contract was awarded in May, 1982 and continued into early 1983.

An important finding of the USAF/DITC and Optotek/DITC contracts was that it was not found practical to construct high-performance, fully-abuttable modules at 125 lines-per-inch resolution; the upper resolution limit currently deemed feasible for expandable display construction is approximately 100 lines per inch. (This corresponds to achieving standard 525 line presentation for screen dimensions of approximately 5"). This limitation is also felt to apply to multicolor LED displays.

Suggestions for future work include the construction of a 100 line-per-inch LED screen based on 0.5"x0.5" or 1"x1" modules; concomitantly the design and acquisition of the necessary complement of custom LSI drive circuits is recommended. Information on the scope and scale of these contemplated projects has been provided to the USAF & DITC.

## 2.0 TECHNICAL

### 2.1 Materials Development and LED Array Fabrication

At the commencement of the video display program Optotek had just completed a Canadian contract involving the development of advanced processing assembly techniques for visual LED arrays. Although this work had concentrated on resolutions applicable to vector-graphic arrays, it was hoped that the developed technology could be extended and applied to higher resolution arrays.

### 2.2 LED Processing (USAF/DITC Contract)

The original rationalization leading to selection of 125 line-per-inch for the resolution of the LED video display is presented in Table 1.

(In the context of the remarks made in the introduction, it is noteworthy that a resolution of 100 line-per-inch could result in adequate video performance for screens of the sizes required for military avionics applications.)

The initial LED design contemplated for the fabrication of 125 lines-per-inch video resolution displays is illustrated in Fig. 1. The circular aperture design was deemed necessary for high luminance performance; contacting of such structures dictates a minimum aperture size of 4 mil diameter; countervailing, the abutability requirement limits this aperture to a maximum of 3 mils. Even this latter dimension imposes severe constraints on junction to chip edge and intermodule dimensions. To allow assessment of trade offs the mask set ordered had provision to accommodate up to 4 mil diode apertures.

125 lines/inch VIDEO LED DISPLAY using 128x128  
element XY addressable 1"x1" abuttable modules

- o Standard North American TV systems use 525 lines. Resolution depends on screen size.
- o Aiming for video resolution in a matrix display for the expected aircraft screen size of about 5"x6" requires  $525 \text{ lines}/5 \text{ inches} \approx 100 \text{ lines/inch}$ .
- o Rounding off to nearest integer binary number to facilitate associated electronics results in 128 lines/inch.
- o Selecting modular building blocks of approximately 1"x1" results in diode centers of  $1000 \text{ mils}/128 \text{ lines} = 7.8125 \text{ mils}$ .
- o Rounding off to 8 mils to be compatible with manufacturing equipment results in modular building blocks of  
$$8 \text{ mils} \cdot 128 = 1024 \text{ mils}$$
- o Resultant resolution becomes  
$$128 \text{ lines}/1.024 \text{ inch} = 125 \text{ lines/inch}$$
- o Note that display resolution for the flat LED matrix display is independent of screen size.

TABLE 1            GENERAL BACKGROUND

Reflow in I.R. belt furnace, to form good contacts.

This experiment was successful in primarily demonstrating that the reflow process was workable.

#### Application to Flip Chip Structures

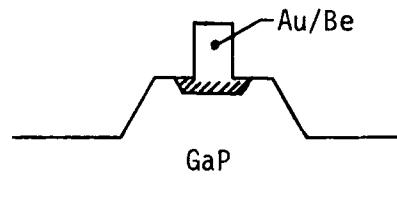
The semi-flip chip (SFC) configuration was selected for evaluation purposes.

This subsection describes the sequence of operations leading to the fabrication of the solder bumps and the results obtained with the procedure modified for mesa etched LPE GaP material in SFC configuration. Although this variant of the bumping process was investigated here for non-planar LPE, it can be assumed it would also work, and probably more easily, in the case of the VPE planar structures.

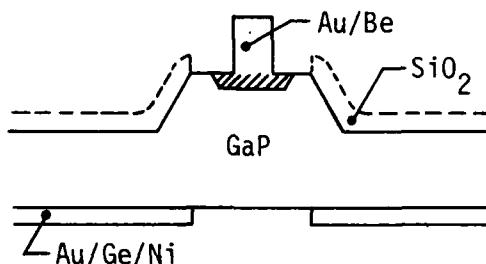
Plating and spheridizing the bumps is accomplished relatively straightforwardly, when the steps of the summary flow chart of Table 4 are observed. Photographs illustrating the appearance of the bump contacts are shown in Figs. 7-9. From Fig. 7 the flow lines achieved after reflowing are distinguishable. In the upper photograph of Fig. 8 (Cu solderable metal) it will be noted that some bumps achieve a spherical configuration during the initial plating process. After reflow (lower photograph) the wafers showed total reflow, but observation under high magnification showed same Cu diffusion into the Pb-Sn. It is therefore necessary to define carefully the conditions (time and temperature) necessary for satisfactory reflow.

Inspection of the photographs of Fig. 9 will show that, in the case of Au, there is no significant difference between the appearance of the bumps before and after flowing. When

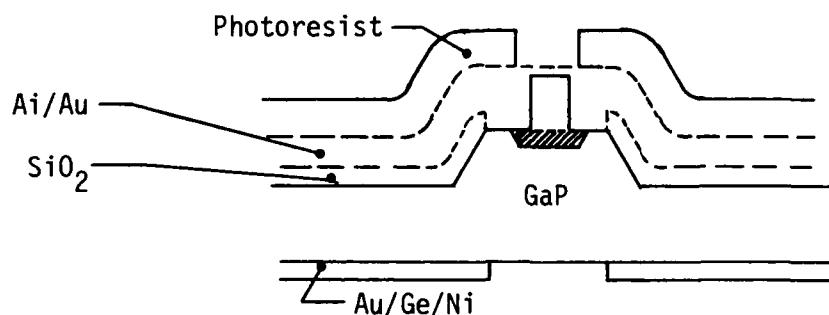
1. Starting material



2. Chemical vapour deposition of  $\text{SiO}_2$  (1000Å) and subsequent opening of the Au/Be windows.



3. Ti/Au evaporation - positive photoresist operation and opening of the Au/Be window covered with Ti/Au.



4. solderable metal plating - Pb/Sn (5%) plating

5. Resist removal

6. Etching of the Ti/Au layer not protected by the Pb/Sn

7. Bumping

8. Spheridizing

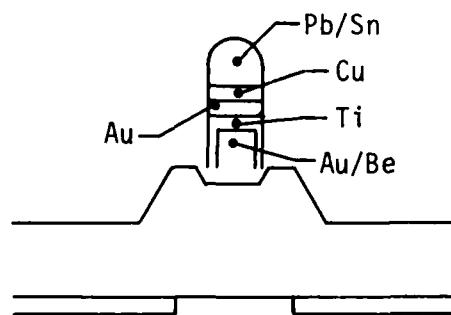


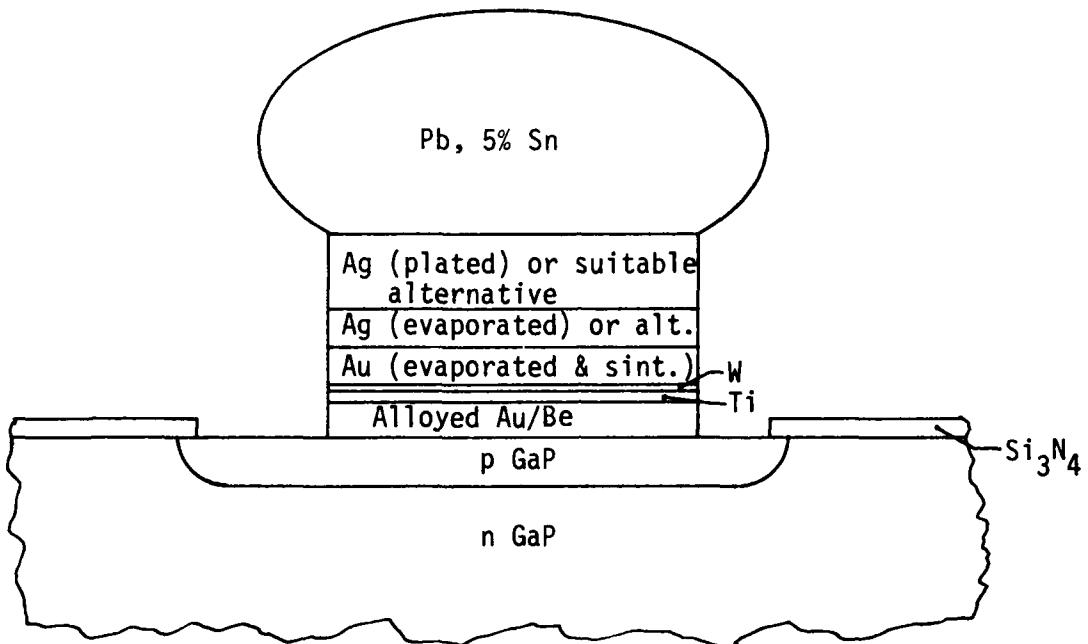
TABLE 4 FLOW CHART - SOLDER BUMP PROCESS (SFC)

- (3) Ag plating onto Ti/Au linked rail or sheet. This needed further optimization to avoid  $H_2$  overvoltage, especially at the start of plating, and to achieve uniform plating. Cu plating was similar to Au plating in its difficulties.
- (4) Au plating had to be carried out very slowly to avoid  $H_2$  overvoltage.
- (5) Pb, 5% Sn plating was achieved into apertures on a Cu plate.
- (6) Spheridizing of Pb, 5% Sn was carried out, but was not tested for reflow.

#### Rail Matrix Check or Reflow Properties

This required:

- (i) Preparation of rails in 1 mil thick Au on ceramic (saw cut)
- (ii) Spheridizing of dots on rails on a semiconductor substrate, with intervening dielectric. This can be prepared as follows:
  - (a) Start with poly Si +  $Si_3N_4$  CVD layers
  - (b) Evaporate Ti/Au
  - (c) Photolith process to give linked rail.
  - (d) Sinter at 400°-460°C.
  - (e) Photolith process to give dot windows in photoresist.
  - (f) Ag electroplate.
  - (g) Pb, 5% Sn electroplate
  - (h) Photoresist strip
  - (i) Spheridize.



Estimated thickness requirements:

Au/Be(e)	3000Å
Ti(e)	500Å
W(e)	100Å
Au(e)	3000Å
Ag(e)	3000Å
Ag(p)	6000Å
Pb, 5% Sn as plated	20000Å (30000Å when spheridized)

(e) - evaporated

(p) - plated

FIG. 6 SOLDER BUMP STRUCTURE

### 2.2.1 Solder Bump Development

In investigating this technology it was recognized that attempts to develop a viable process were limited by the fact that the following equipment was not available at Optotek:

- E-gun evaporator with multiple source
- Sputter system with multiple source
- Pd evaporation/electroplating process

Investigations concentrated on what could be achieved with available equipment and materials. Success would point the way towards an economical production method, which would likely require the acquisition of additional, specialised equipment if significant volume is required.

The anticipated solder bump structure is depicted in Fig. 6. Initial experiments were conducted using planar-junction VPE material.

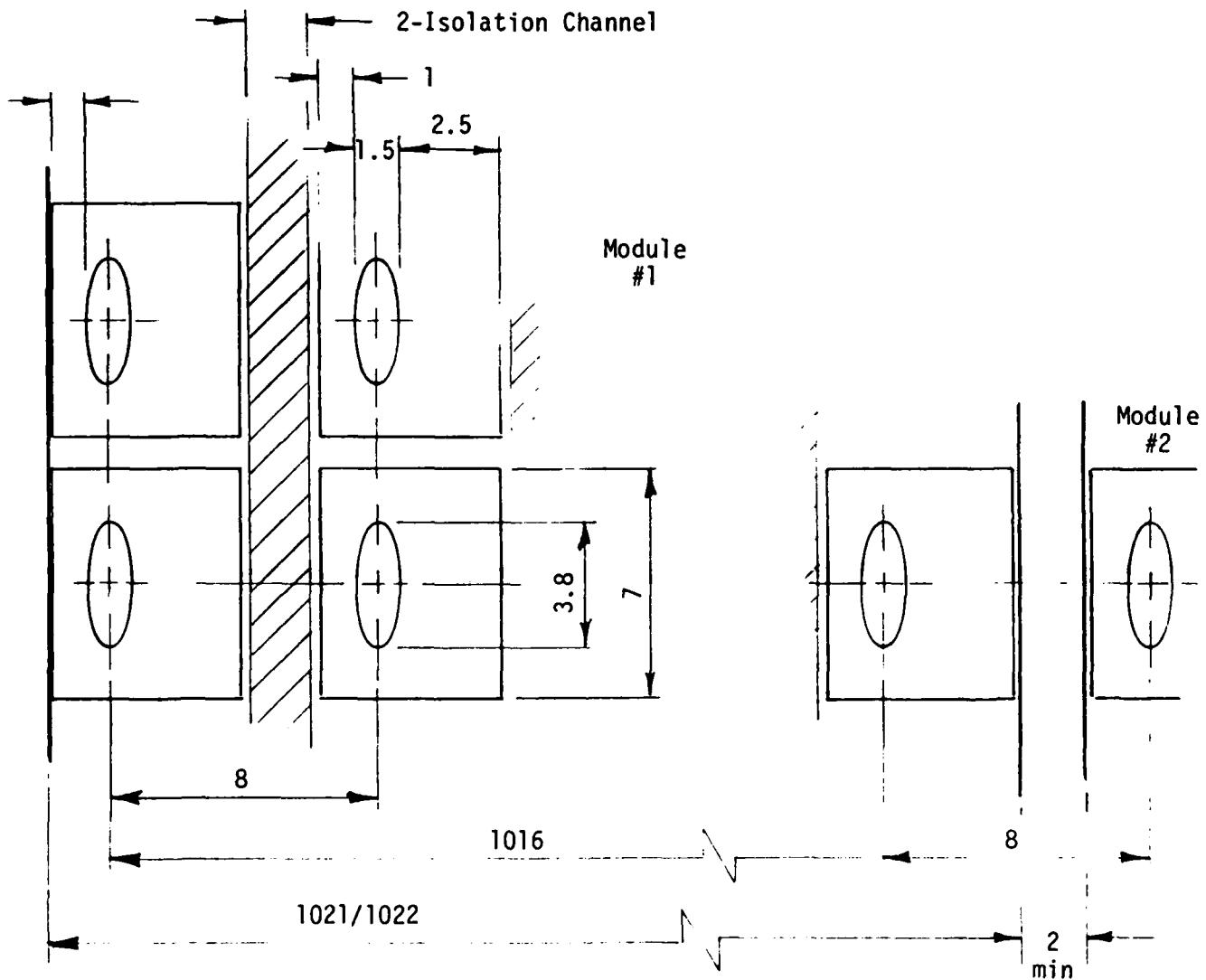
Process procedures deemed to be understood and under control are summarised below:

- (1) Ti evaporation This was carried out from a W filament with probably an increasing concentration of W towards the upper surface of the evaporated Ti. Au was then evaporated in situ.
- (2) Au and Ti etch The Au etch was basically KI but a few seconds in buffered HF were sometimes required to clear traces of W evaporated from the filament. The W and Ti, from the Ti evaporation, was subsequently etched in buffered HF. It was difficult, however, to determine completeness of Ti etching.

assembly confirmed that, in the case of SFC & SSB, more real estimate was needed between LED junctions to allow enough space for the required edge connections. In May, 1981, a new mask set for an oval LED was initiated (Fig. 5); this increased junction spacings in one direction without further reducing the emitting area. In the same time frame the design of fixtures and test equipment to handle the 1"x1" array was initiated.

Full flip-chip (FFC) still appeared to offer the best hope for high-resolution array construction; a major advantage is the planar viewing surface free from electrical connections and sawcuts; this facilitates contrast enhancement. Moreover, since both anode and cathode FFC connections are made on the substrate side, module abutment is greatly facilitated. Unfortunately, prior to the mid-point of the contract difficulties were experienced in obtaining insulating GaP substrate. Chromium-doped (insulating) GaP substrate was used for previous FFC work (for example, the Canadian advanced display development contract completed mid-80). At that time the material was available from Monsanto and UK/Japan sources. These sources subsequently stopped manufacturing due to program reorientation (Monsanto/GI transition) or lack of demand. In early 1983 Optotek finally identified an alternative European source of insulating GaP; samples were evaluated and appeared suitable for the application. Unfortunately, this prospective solution did not materialise at a point where it was still feasible to contemplate the use of such a procedure. Other approaches to FFC implementation which obviate this requirement could be used - for example, solder bumping of contacts or the use of multi-level metallization on the surface of the LED, the latter permitting bonding on wider centers; both would have involved further development work to a level well beyond the scope of the program. (Information on solder bump technology development as investigated during the time frame of the contract is presented in the following subsection.)

125 LINES PER INCH VIDEO LED DISPLAY



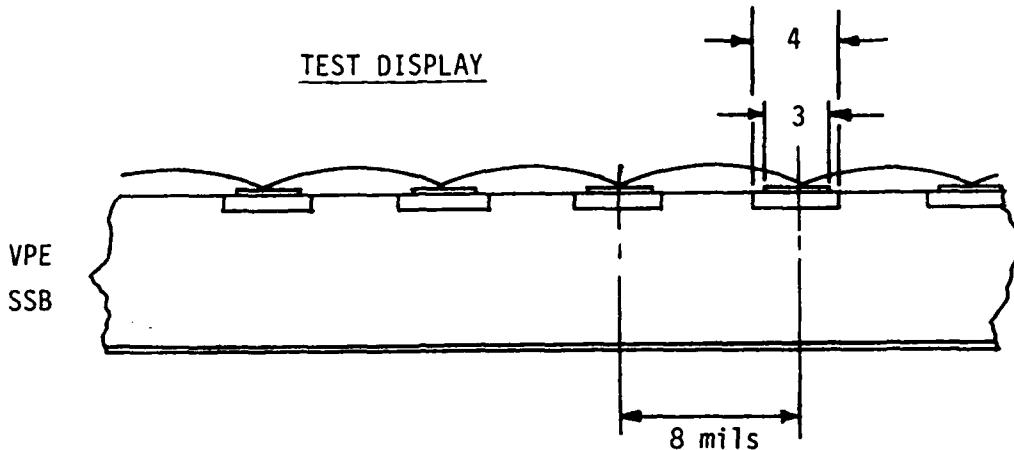
Note: Dimension in mils.

FIG. 5 OFFSET PATTERN CONCEPT

125 LINES/INCH VIDEO LED DISPLAY

TEST DISPLAY

o STRUCTURE



o CHIP SIZE

32x32 element building blocks.

o LUMINANCE

$L_v = 35$  FL @ 16mA, 1/128 duty cycle averaged over a 6 mil diameter pixel area.

o USAGE

1. Refinement of mechanical isolation and bonding techniques on 8 mil centers.
2. Test load for system integration of TV camera, decode/drive electronics, and LED array.

TABLE 3 TEST DISPLAY DATA

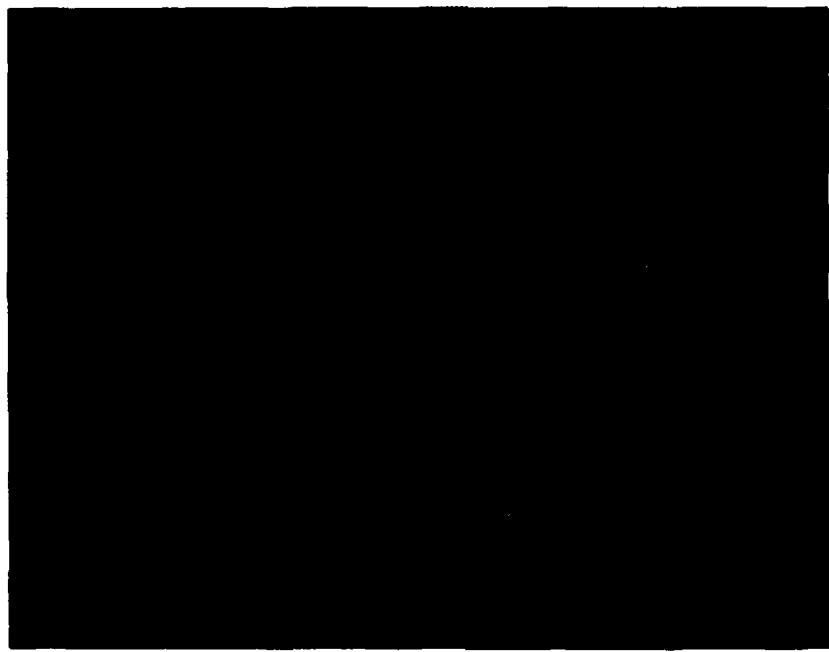


FIG. 4 VIDEO-RESOLUTION EVALUATION DISPLAY

125 lines/inch VIDEO LED DISPLAY

Performance

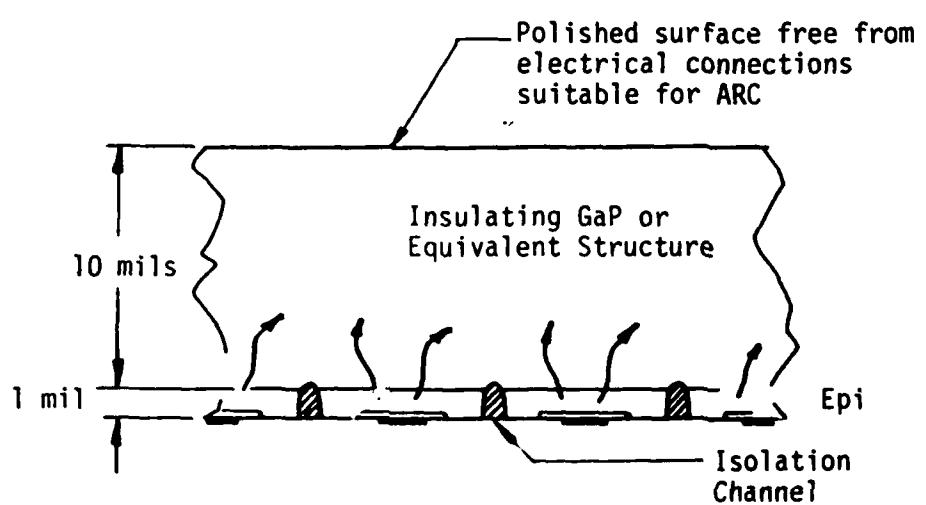
Optimistic extrapolation of luminance values achieved with SFC for 8 mil diameter emitting apertures on 16 mil centers is presented in tabular form below.

VIDEO				MMM
1/8 mA Ave. or 16 mA @ 1/128 D.C.				1mA Ave. or 64mA @ 1/64 DC
GREY SCALE	$I_v$ ( cd)	$L_v$ (FL) 3 mil dia.	$L_v$ (FL) 3 mil on 8 mil d	$L_v$ (FL) 8 mil dia.
8	24	1600	180	1800
4	12	800	90	900
2	6	400	45	450
1	3	200	23	230
0	0	0	0	0

Note that some rounding of numbers has been introduced.

TABLE 2 VIDEO LED DISPLAY PERFORMANCE

125 lines/inch VIDEO LED DISPLAY



Available Techniques

for

Isolation

Diffusion  
Etched channel  
Sawcut

Interconnection

Bilevel metallization  
Epoxy/Solder bumping  
Stitch bonding

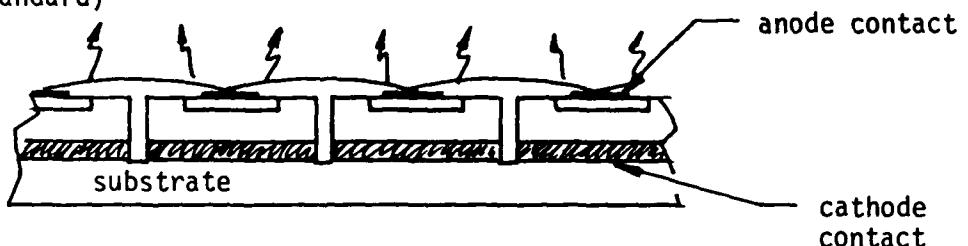
Selection of the most practical combination of above has not yet been made.

FIG. 3 ANTICIPATED FFC STRUCTURE

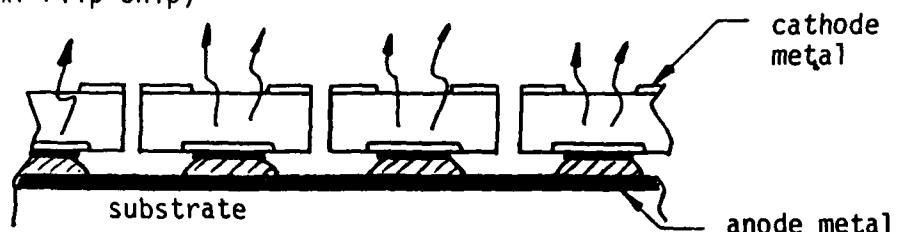
## 125 lines/inch VIDEO LED DISPLAY

- o The mask set ordered allows for 3 different LED designs with allowance for size variations in each of these 3 designs.

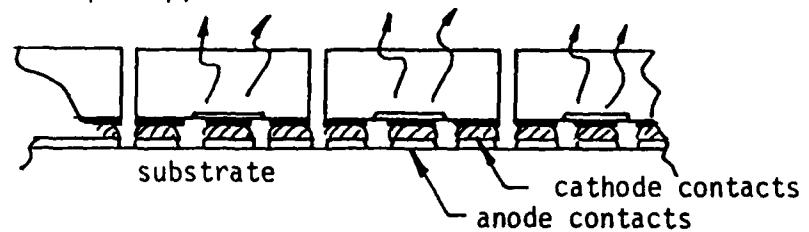
- o STD (Standard)



- o SFC (Semi-Flip Chip)



- o FFC (Full-Flip Chip)



- o Since both STD and SFC have electrical contacts on two sides, viewing side electrical connections must be made from front to rear. The tight LED spacing appears to prohibit adequate connections. Both edge type and inboard connection have been considered.
- o FFC with both anode and cathode contacts in the rear appears to have the best chance of success.

FIG. 2 ELECTRICAL CONNECTIONS VS. LED DESIGN

The three LED configurations contemplated for LED array construction were:

- Standard Stitch Bond (SSB)
- Semi Flip Chip (SFC)
- Full Flip Chip (FFC)

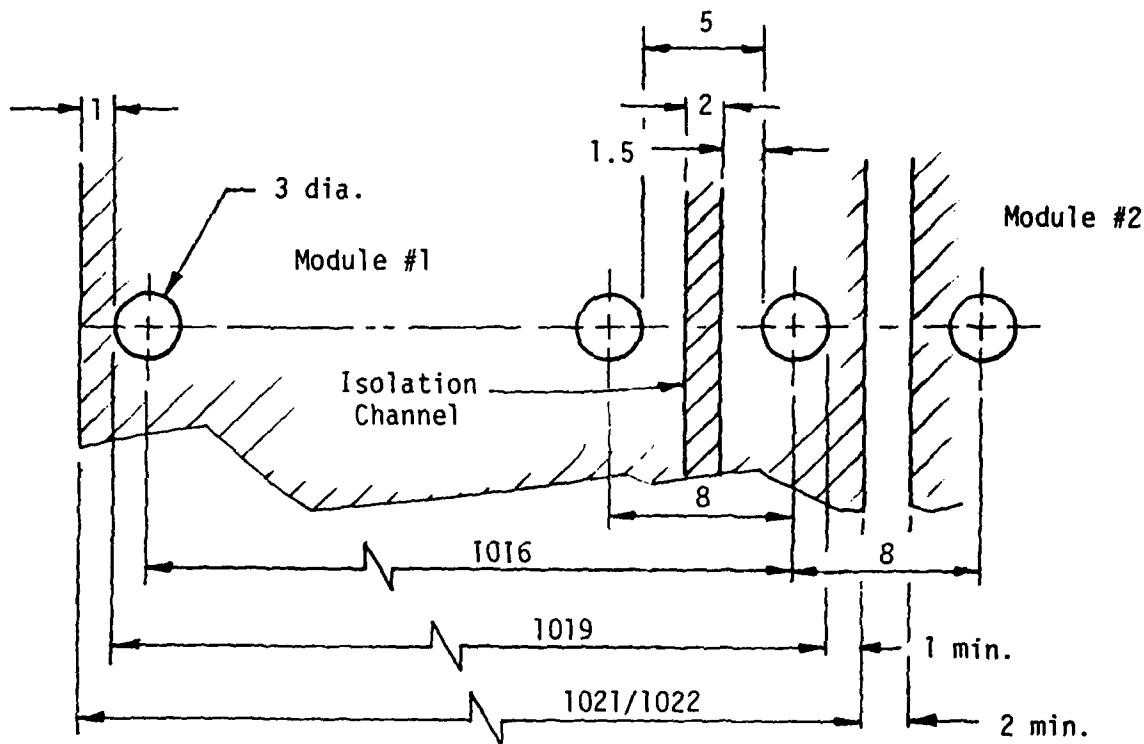
These different configurations are illustrated in Fig. 2. Because both SSB and SFC configurations require electrical connection from the viewing surface to the rear of the array, the FFC designs, with all contacts on one face, offered advantages. (This technology had been investigated in some detail during both the original Multimode Matrix contract and also the subsequent Canadian contract referred to above. Certain difficulties had been experienced in productionizing FFC designs, and it was not clear at program commencement if the technology could be used for video array fabrication.) The alternate approaches to achieving the FFC configuration are illustrated in Fig. 3.

The initial performance estimates for video LED displays are presented in Table 2.

The first video resolution test array was delivered to the USAF in December, 1980. This demonstrator involved a partial array plus associated electronics. A rechargeable battery was provided to facilitate demonstration. The array was built using vapor-phase epitaxial material. Light-output performance was not at a sunlight visible level, instead being more representative of MMM prototype performance. It did, however, demonstrate the achievement of the necessary resolution in green-emitting GaP material. Fig. 4 is a photograph of the display surface and Table 3 presents performance data.

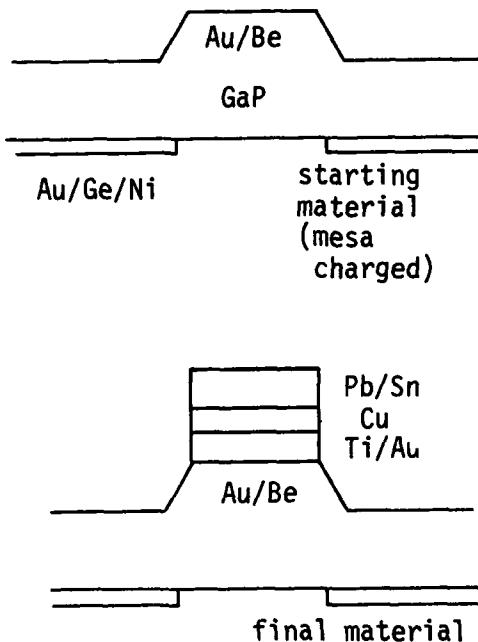
In the early phase of the contract three different LED configurations were produced on 8 mil centres (125 lines per inch) - FFC, SFC & SSB. All emitting apertures were circular. Trial

125 lines/inch VIDEO LED DISPLAY



- o Circular emitting area based on luminance enhancement techniques.
- o Maximum emitting aperture diameter allowing abutment without loss of resolution appears to be 3 mils.
- o Mask set design can accommodate diameters up to 4 mils.

FIG. 1 ABUTMENT VS. EMITTING APERTURE SIZE

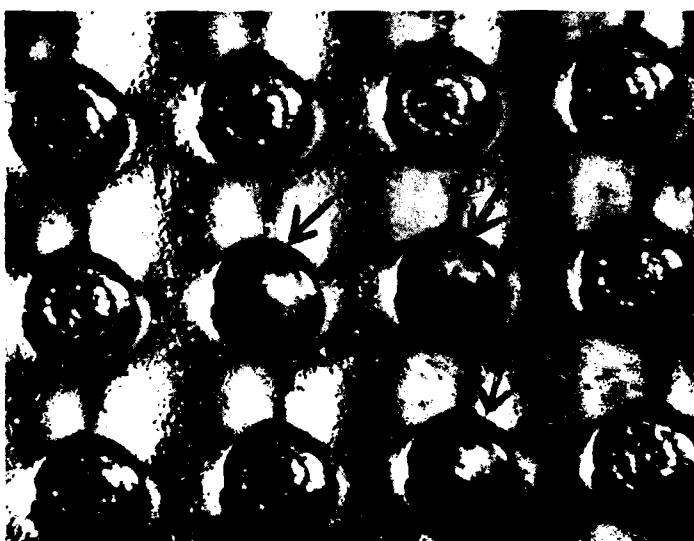


Final material before reflowing

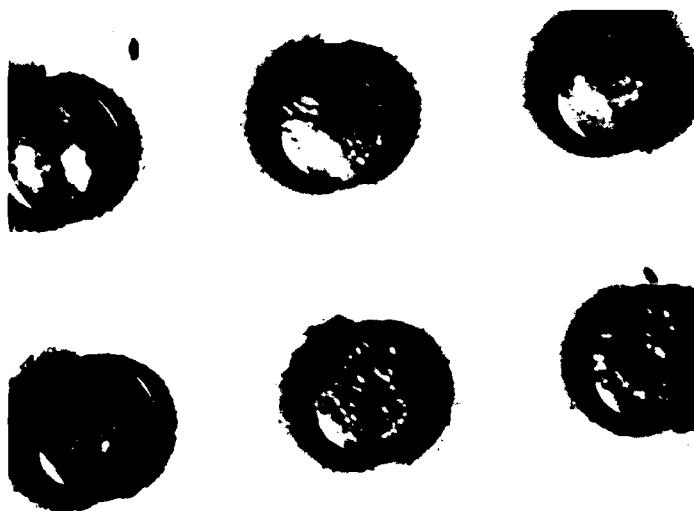


Final material after reflowing

FIG. 7 SOLDER BUMP PROCESS



After 1st reflowing cycle  
the arrow-noted bumps are  
totally reflowed.

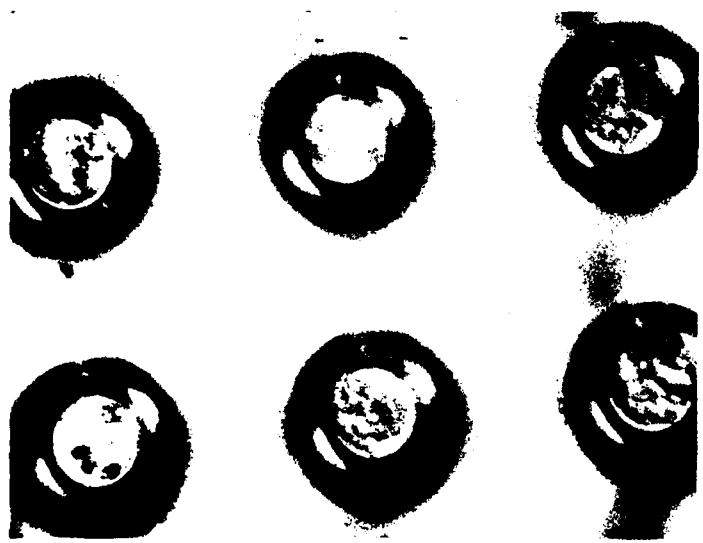
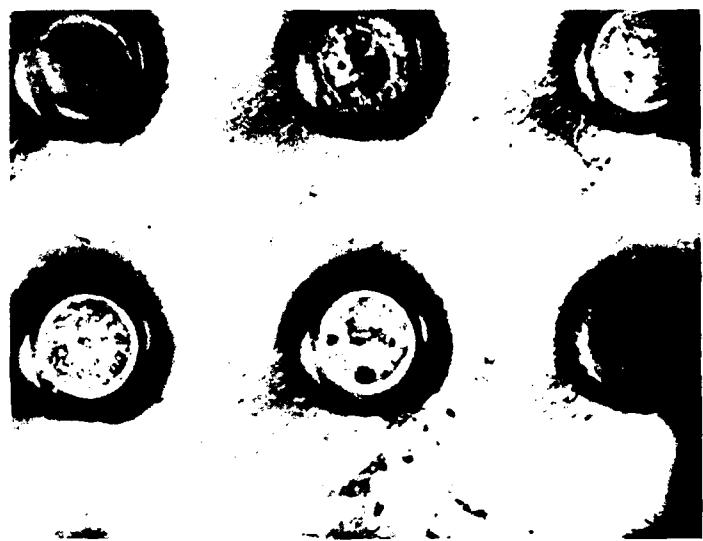


After second reflowing cycle  
the wafers are totally reflowed,  
but from microscope observation  
(high magnification) it may be  
seen that the Cu diffusion into  
the Pb/Sn starts to be too  
important. It is then necessary  
to define carefully the time and  
temperature of reflowing (more  
or less time, more or less  
temperature).

Reflowing Temperature and Time

Solderable Metal = Cu

FIG. 8 SOLDER BUMP PROCES (CONT'D)



Solderable Metal = Au

FIG. 9 SOLDER BUMP PROCESS (CONT'D)

Au was used as the solderable metal it was noted that Pb-Sn-Au thermal interdiffusion is also induced by the plating electric field when the Pb-Sn alloy was plated over the solderable Au. Ag was intermediate between Cu and Au in terms of interdiffusion effects.

In addition to metallurgy, the electrical characteristics of the solder-bump contacts were evaluated.

The main results are summarised below:

- (a) The plating and spheridizing process did not degrade the forward voltage  $V_F$ 's of the diodes.
- (b) Cu was the best solderable metal in terms of metallurgy and selected properties, followed by Ag. Au was the least satisfactory.

#### Conclusions

The basis for a solder bump process has been established.

Additional work deemed necessary, but not conducted during the time frame of the contract is summarised below:

- (1) Obtaining plating uniformity for rails and plated 95:5 Pb/Sn
- (2) Alignment and jigging of semiconductor to ceramic rails.
- (3) Reflow time-temperature for 95:5 on different metals, contacting different rails.
- (4) Evaluate the use of a  $H_2$  torch for rework of these metal systems.

- (5) Etching solderable metal without attacking the Pb-Sn bumps.

Further significant development would have been required to refine the process in application to video resolution arrays. Additional equipment would also be required.

In connection with future work in this area, consideration should be given to licensing existing solder-bumping processes (IBM's).

#### 2.2.2 Deliverable Array

The relative merits of the three array construction techniques as determined in mid 1981 is summarised in Table 5. Performance projections are presented in Table 6.

For resolutions of 128 lines per inch, it was determined that abutable arrays could only be achieved by either:

- (i) Oval-junction, offset SSB
- (ii) Full FFC

The former is not compatible with sunlight visibility performance. The latter requires further development work related to interlevel metallization and bump contact technology; but the associated effort was beyond the scope, time-frame and funding of the existing video contract.

In mid 1981 the decision was taken to build the first 1"x1" module using SSB and to concentrate on SFC for higher luminance performance; the SSB array was not abutable but was intended as a test array to gain further experience with isolation and bonding on the tight 8 mil centers.

### 125 LINES/INCH VIDEO LED DISPLAY

3 LED structures have been evaluated.

- o Standard Stitch Bond (SSB)
- o Semi Flip Chip (SFC)
- o Full Flip Chip (FFC)

#### SSB

- o Simple Processing
- o High Yield
- o Relatively Low Luminance
- o Oval offset LED junction deemed necessary to achieve abutability
- o 128x128 element test array being constructed to gain isolation and bonding experience on 8 mil centers
- o Requires over the edge connections for abutability

#### SFC

- o More Complex Processing
- o Lower Yield
- o High Luminance
- o Small or oval LED junctions deemed necessary to achieve abutability
- o Requires over the edge connections to achieve abutability

#### FFC

- o Most Complex Processing
- o Lower Yield
- o High Luminance
- o Both anode and cathode contacts on the rear surface eliminating the need for over the edge connections, however X-Y interconnections difficult on 8 mil video resolution centers.

TABLE 5 VIDEO LED DISPLAY STRUCTURES

<u>Device Type</u>	<u>Comparative L<sub>v</sub></u> <sup>†</sup>
SBS	100
SFC (VPE)	100
SFC (VPE/LPE)	400
FFC VPE	100
FFC VPE (Luminance enhanced)	150-300
FFC (VPE/LPE)	400
FFC (VPE/LPE) (Luminance enhanced)	600-1200

<sup>†</sup>Based on 6 mil emitting area and 16mA 1/128 DC.

TABLE 6 REPRESENTATIVE DATA FROM SAMPLE  
VPE ARRAYS

One significant potential advantage of Planar-processed SSB VPE material is the relatively high yield achievable. This is illustrated in Fig. 10 where the feasibility of selecting full 1" x 1" monolithic blocks is demonstrated.

Performance data on sample arrays in the various configurations evaluated is presented in Table 7.

In September 1981 the SSB test array was completed and integrated with the demonstration electronics (Section 2.2). Subsequent to directives generated at the PRG held that month work was initiated on a 128x128 element SFC array. Although this configuration is difficult to implement for four-edge abutable units, two edge abutability appeared feasible. (Two-edge abutable arrays could still be used to produce a number of screen sizes).

At this juncture the USAF/DITC funding allocation became depleted. Work continued on processing and assembly of the 128x128 SFC array using company funding pending award of a supplementary Optotek/DITC contract to permit completion of this work. (Section 3.0)

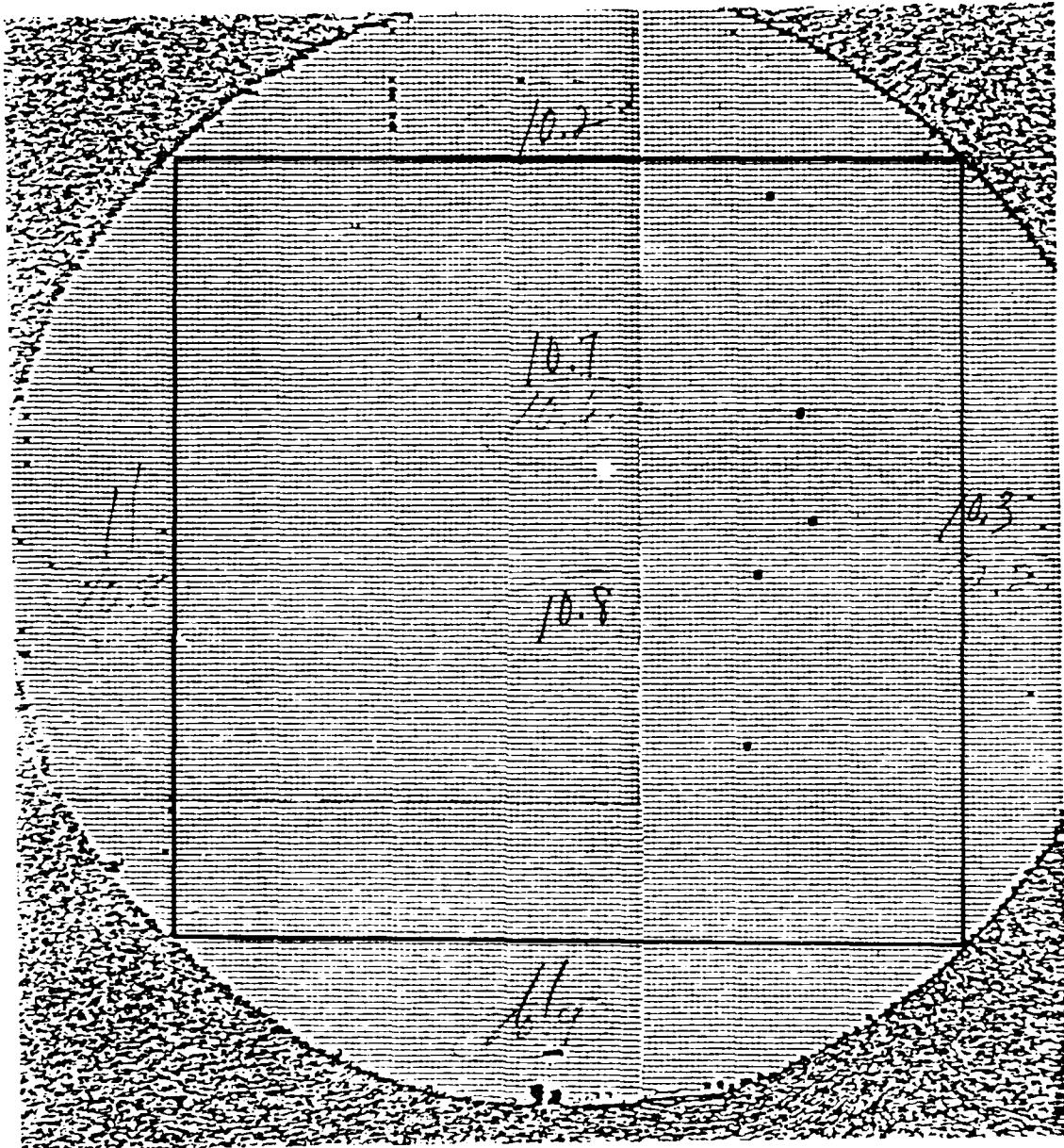
As discussed earlier, an 18x32 SFC array was constructed to demonstrate that the sunlight visibility requirements of the statement-of-work could potentially be achieved in this configuration. Configuration and typical comparative results are presented in Fig. 11.

### 2.3 Array Package

Special ceramics were fabricated to accommodate the various sample arrays and the 1" x 1" SSB video array. The associated thick film work was conducted in-house.

The array interconnect configuration is illustrated in Fig. 11.

125 LINES/INCH VIDEO LED DISPLAY



Fully monolithic

128x128 element LED array made from a single wafer, 4 mil diameter junctions on 8 mil centers

5 random defects out of 16384 LED's (0.03%)

FIG. 10 VIDEO LED DISPLAY WAFER

Summary of Video Evaluation Sample Performance\*

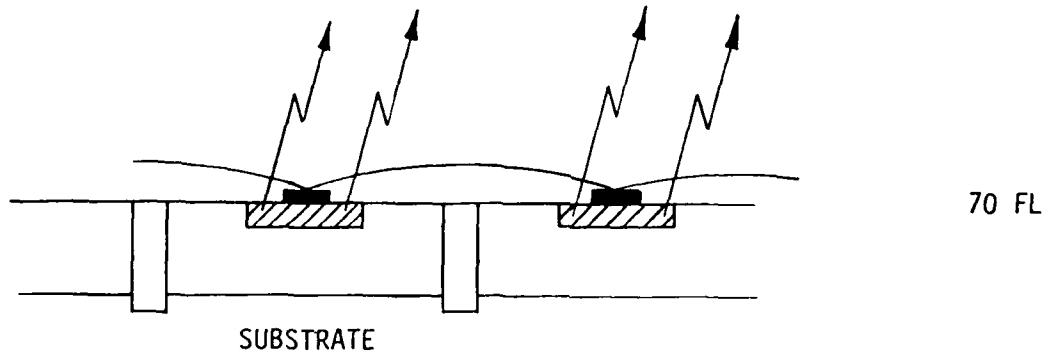
Run #	Array Type	Emitting Aperture in.	Luminous Intensity 10mA dc $\mu$ Cd	Luminance 10mA @ 1/128 Duty Cycle (Derived from 10mAdc measurement)		$V_F$ 10mAdc	$V_R$ 100mA	$R_D$ 10/20mA ohms	$\lambda_p$ (Half Max) $\text{\AA}$	Remarks
				Luminance 10mA averaged over a 0.006" diameter aperture	10mAdc @ 1/128 Duty Cycle (Derived from 10mAdc measurement)					
281	SSB (VPE)	0.006	270	5000	60	2.20	100	20	5630	
282	SFC (VPE)	0.004	300	6000	70	2.10	85	25	6290	
283	SFC (VPE)	0.004	160	3200	40	2.30	66	26	5620	
296	SFC (V/LPE)	0.004	1200	20000	250	2.15	77	18	5640	
304	FFC (VPE)	0.004	200	3600	45	2.20	116	21	5620	
325A	FFC (V/LPE)	0.006	700	12000	150	2.20	80	20	5640	
325B	FFC (V/LPE)	0.006	920	15700	200	2.15	70	20	5640	Luminance Enhanced Structure

\*Without coating or encapsulation.

TABLE 7 SUMMARY VIDEO EVALUATION SAMPLE PERFORMANCE

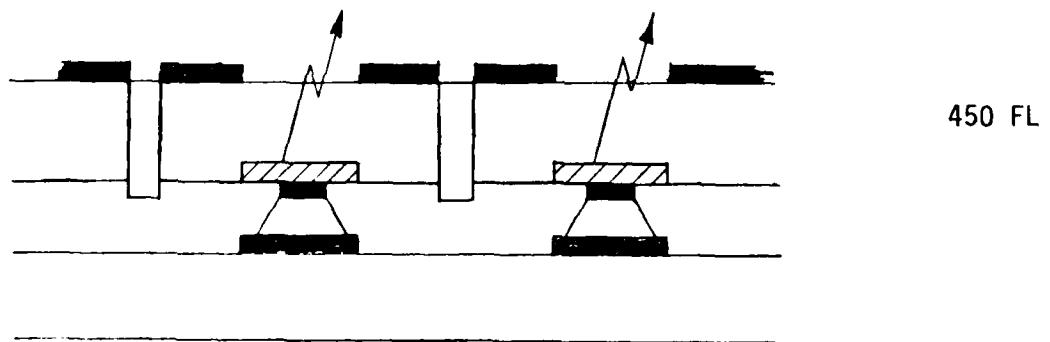
VIDEO DISPLAY PERFORMANCE SUMMARY AT  
1/8MA AVERAGE AND 6 MIL DIAMETER PIXEL

128x128 SSB



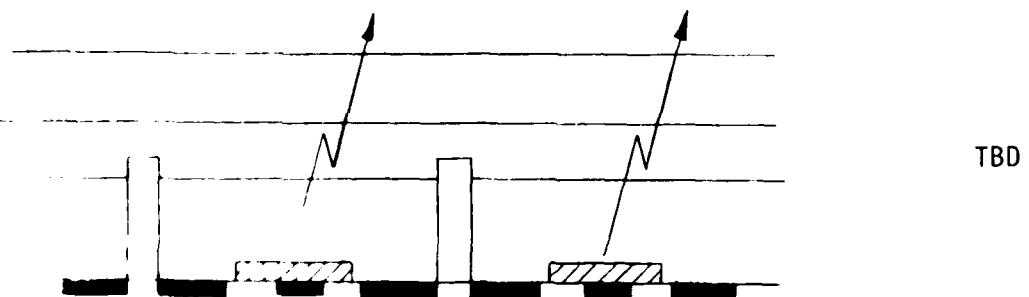
70 FL

18x32 SFC



450 FL

18x32 FFC



TBD

FIG. 11 VIDEO DISPLAY PERFORMANCE SUMMARY

The original display enclosure concept is illustrated in Fig. 12. This was subsequently modified to permit mounting of the array in the vertical rather than horizontal plane to better comply with SOW requirements.

The interconnecting circuit boards as used for the final demo system are shown isometrically in Fig. 13.

#### 2.4 Demonstration Electronics

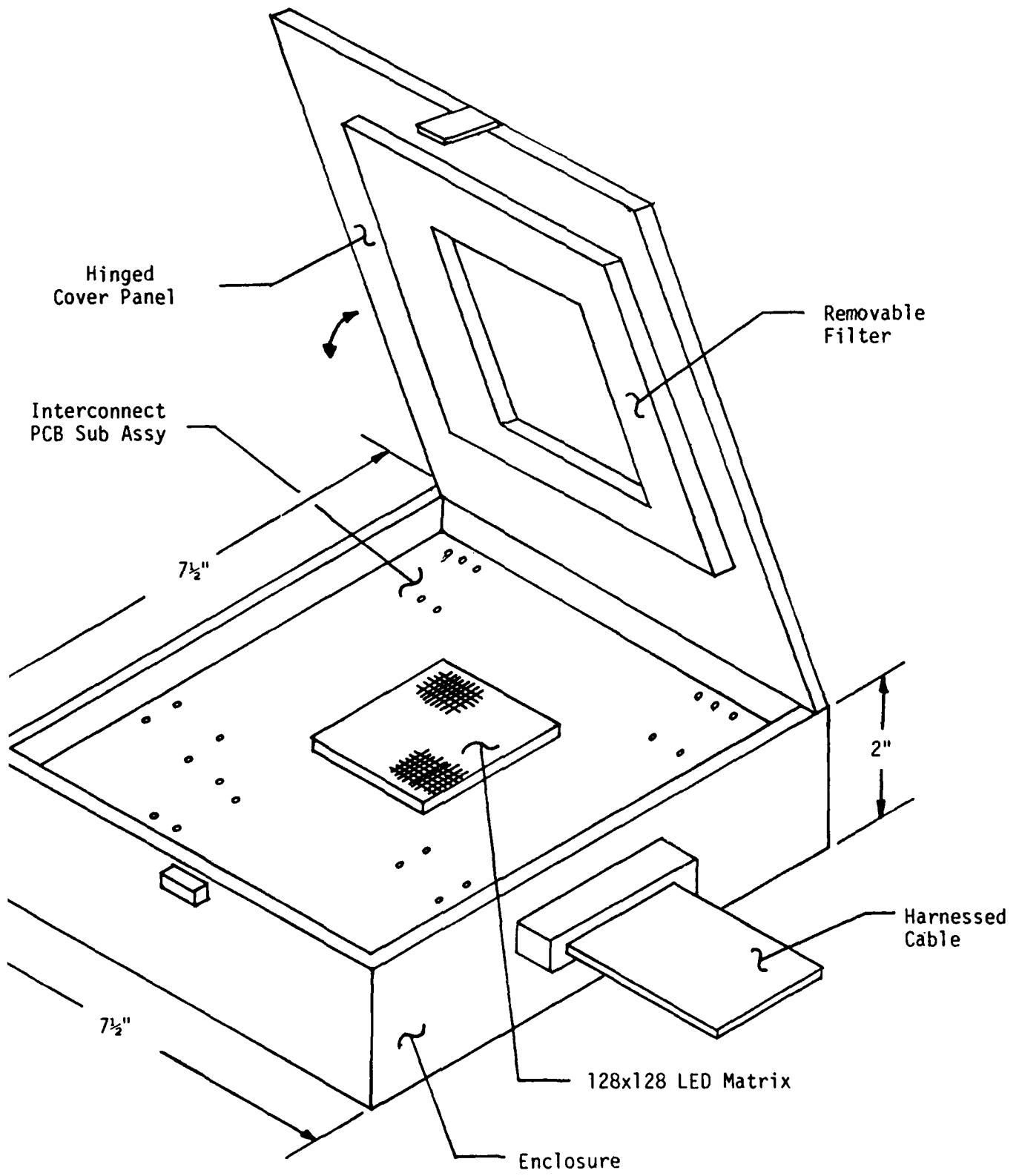
The original LED drive conditions deemed necessary to achieve the video array performance designated in Table 2 are detailed in Table 8.

The initial demonstration electronics block diagram is presented in Fig. 14.

Optotek's original grey-scale implementation concepts were modified (Fig. 15) after a December 1980 meeting with the USAF; these modifications provided the capability to use seven shades of grey above zero; the Program Review Group participants felt that this expanded grey-scale capability would be necessary to justify any subsequent investment relating to the design and development of custom integrated drive circuits. Brightness control with tracking grey scale was also deemed necessary. Figs. 16 and 17 explain how the grey scale is configured to give seven shades with a  $\sqrt{2}$  ratio. Brightness control with tracking grey scale was implemented as shown in Fig. 18.

Variable grey scale ratio can be implemented by modifying the grey scale definition decoder.

Drive electronics as finally implemented is shown in Fig. 19.



Optotek Ltd. 128x128 Element Video Resolution Display

FIG. 12 VIDEO DISPLAY ENCLOSURE

125 LINES/INCH VIDEO LED DISPLAY

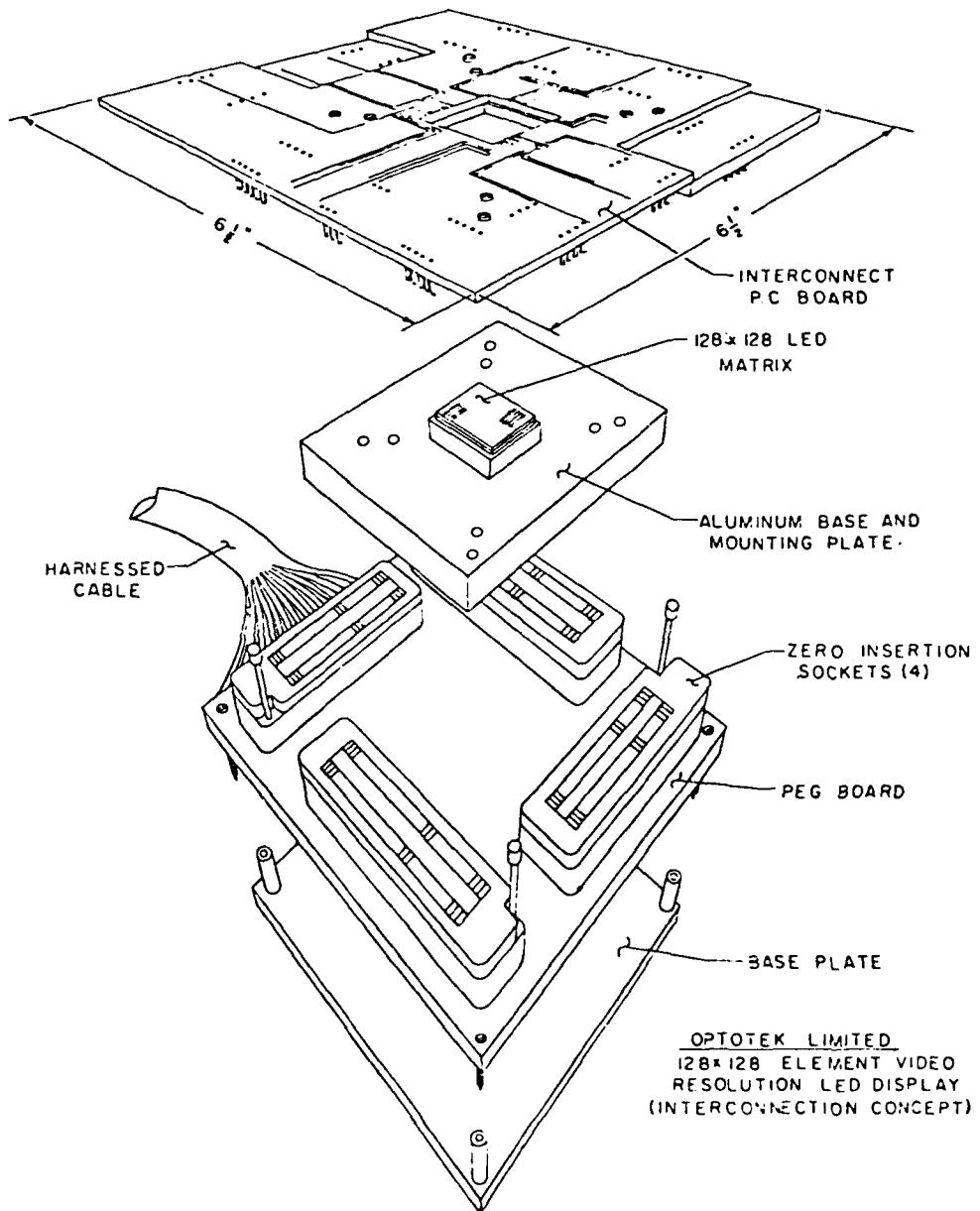


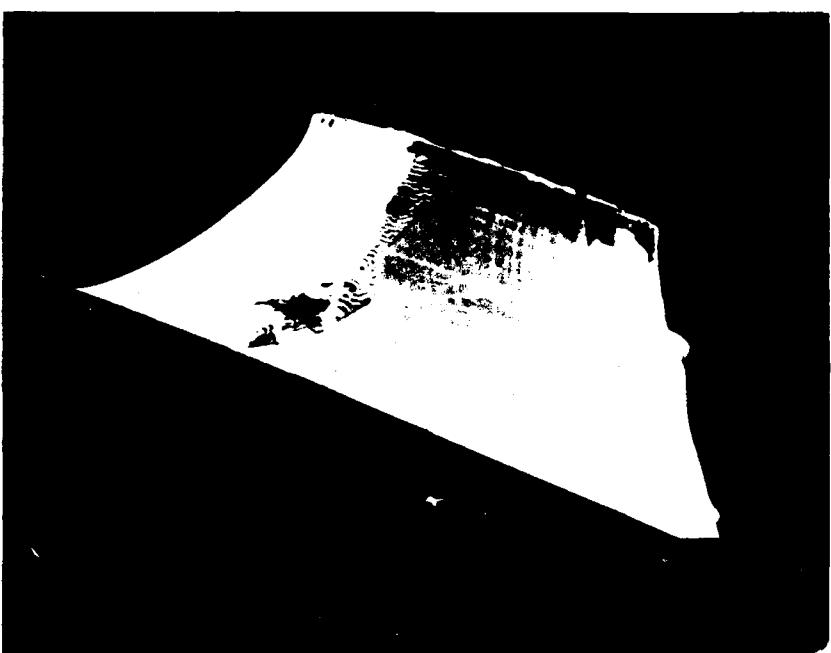
FIG. 13 VIDEO DISPLAY DEMONSTRATION  
DISPLAY INTERCONNECTION CONCEPT

Scanning Electron  
Micrograph of  
Processed SFC Material

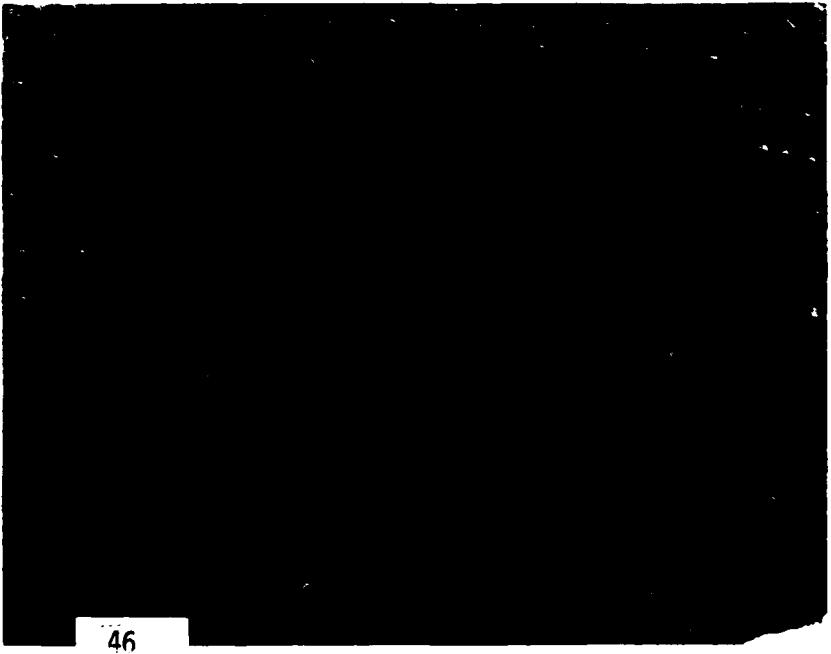
(a)  
SFC mesa (junction  
surface)



(b)  
SFC mesa profile



(c)  
Aperture (cathode)  
surface



### 3.0 SUPPLEMENTARY OPTOTEK/DITC PROGRAM

This program constituted an extension of the USAF/DITC effort and was directed towards building an improved performance 1"x1" semi-flip chip (SFC) array. As discussed in an earlier section, it was understood that this array would only be abutable on two edges.

The Company/Canadian Government program was initiated in October 1981 with the principal effort conducted subsequent to contract award in June 1982.

Ceramic carriers suitable for the 1"x1" SFC array were designed and fabricated. LED material was processed and tested.

Fig. 23 contains scanning electron micrographs depicting the bottom (junction) and top (cathode contact) surfaces of a typical material section. Typical performance data is presented in Table 9 confirming the potential for sunlight visibility.

Optotek's previous experience of assembling SFC material had involved the construction of 1"x1" modules at 64 lines-per-inch. At this vector-graphic resolution the procedure had proved quite successful. A different situation was encountered with 8 mil center material.

Intensive effort was applied to assembling the SFC video material. Both the elapsed time - 2 months, and man-hours required - 1000 hours, greatly exceeded expectations. The principal time consuming factor was associated with ensuring the individual epoxy bumps made satisfactory contact to the anode rails. Contact integrity is adversely affected by any warp in the carrier or monolithic chip plus height variations of individual mesas. In addition, despite the fact that epoxies and curing cycles were selected to best allow sequential curing of mounted chips, contact properties may change during successive curing cycles, resulting in uniformity variations. The compounding of these effects resulted in a high level of rework - and one which was disproportionately high in comparison with previous experience of 64 line-per-inch 1"x1" SFC arrays.

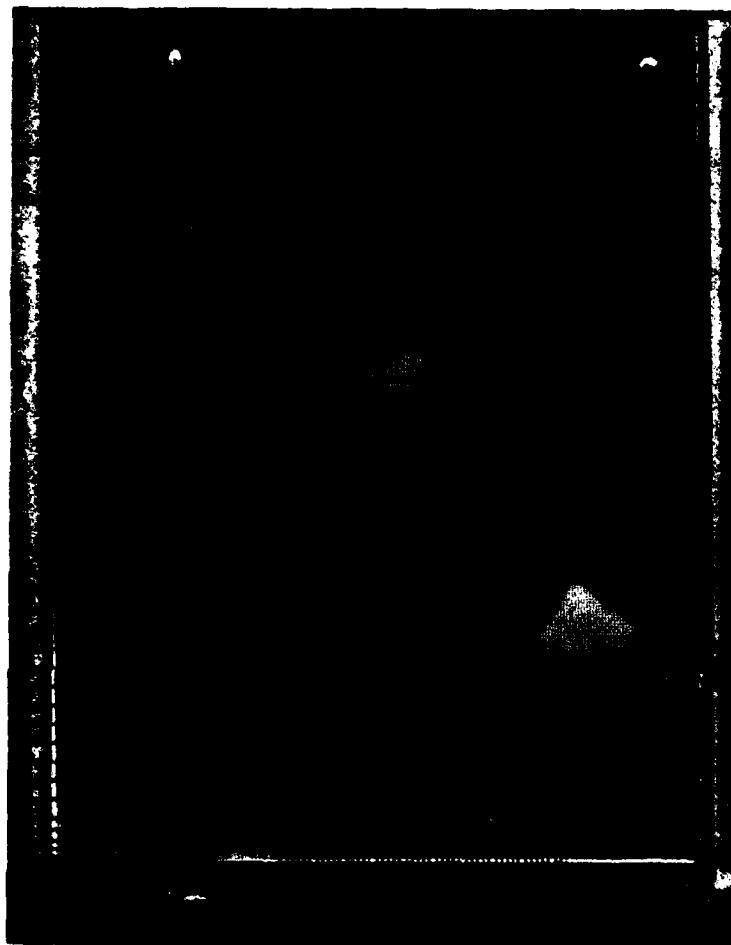


FIG. 22 TYPICAL VIDEO PRESENTATIONS



FIG. 21 TYPICAL VIDEO PRESENTATIONS

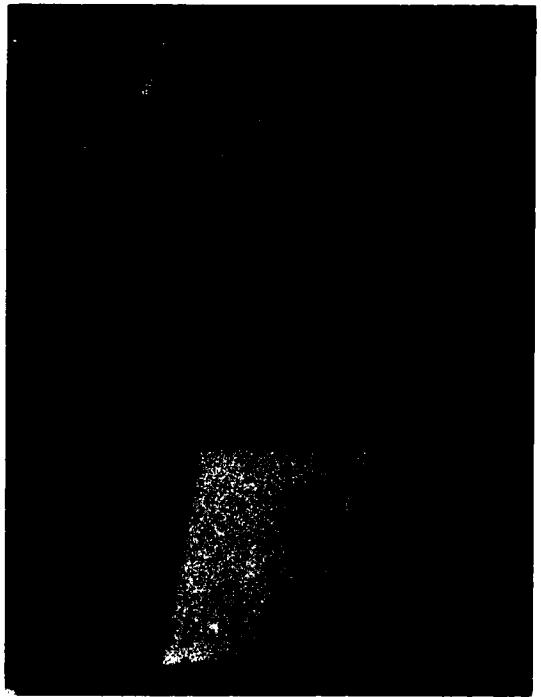
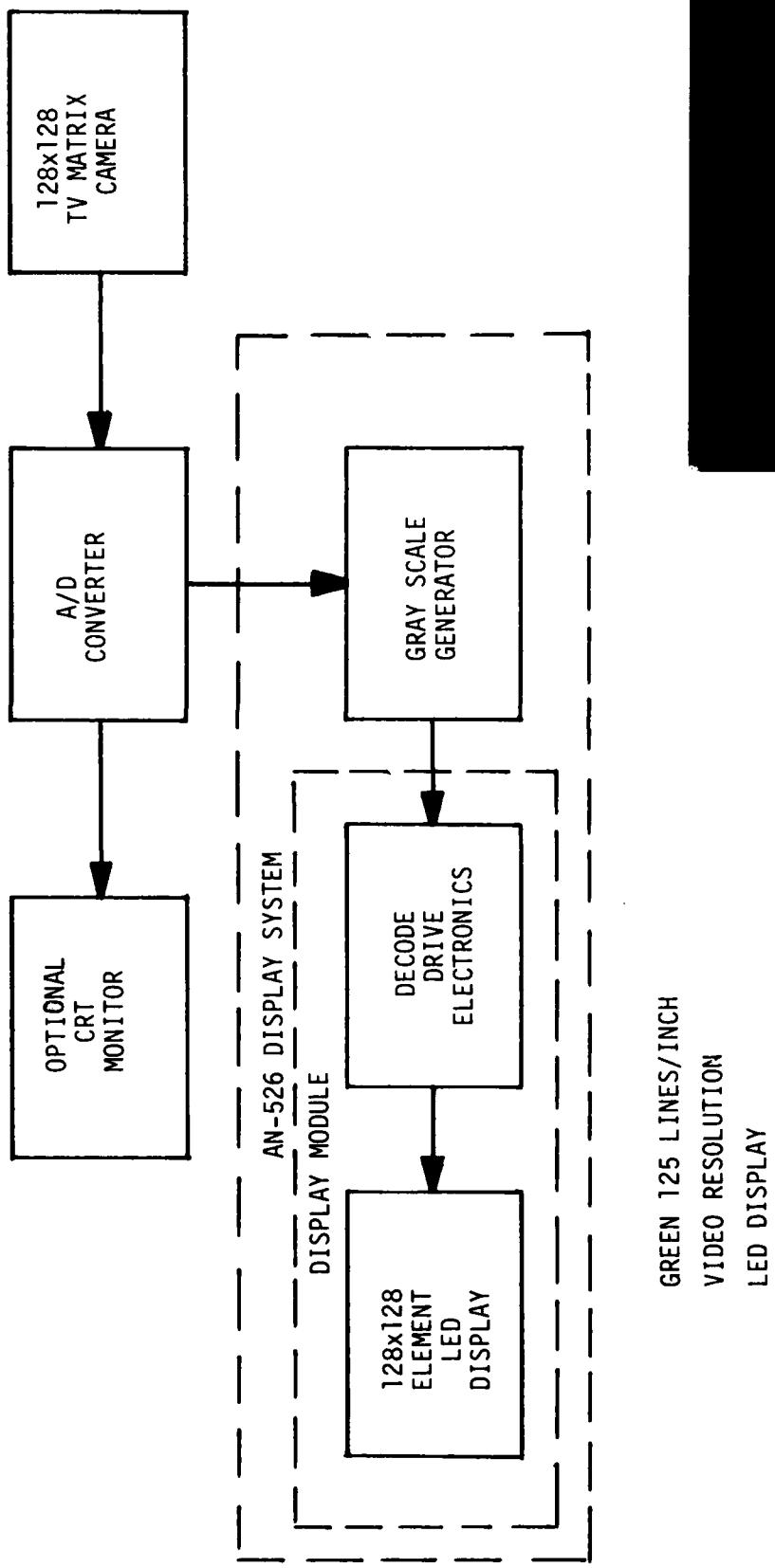


FIG. 20 DELIVERED SYSTEM ORGANIZATION

Given that the Reticon 256x256 500 Hz camera was expected to become available in 1981, the USAF adopted Optotek's recommendation to use a GE 128x128 element 50 Hz camera. The use of the larger matrix was preferred at the expense of lower than 500 Hz frame-rate. Despite the low frame rate the initially conceived system organization and LED duty cycle were retained. Unfortunately GE were unable to meet their original framerate specification and the camera delivered to Optotek only operated at 30Hz. The noticeable flicker obviously has a deleterious effect on system performance. (A 128x128 500 Hz Reticon has recently been announced and the USAF is understood to be considering purchase of this camera.)

The final demonstration system as delivered to the USAF on July 1983 is shown in Fig. 20. Typical TV pictures obtained using this system in conjunction with the 125 line-per-inch SSB array are shown in Figs. 21 and 22.\*

\*These pictures were taken before the array was reworked prior to delivery to the USAF. Defect levels on the delivered system were lower, thereby improving presentation quality.

Considerable effort was expended on identifying the most suitable TV camera for use with the demonstration system. The identified option were:

<u>Matrix</u>	<u>Frame Rate</u>	<u>Manufacturer</u>
100x100	500 Hz	Reticon
256x256	500 Hz	Reticon
128x128	50 Hz	General Electric
244x190	240 Hz	Fairchild

From above summary, Reticon's upcoming 256x256 model looked the most interesting since both the 128x128 organization (every other bit) and the 500 Hz frame rate could be satisfied. This camera could also be used to provide video signals to four 128x128 LED arrays making a 2"x2" screen possible at the 500 Hz frame rate, but at reduced duty cycle.

It was originally expected to be available June 1981, but to date has not been produced.

Alternatives considered and discarded after detailed review with the USAF were:

- 100x100 element video presentation on a 128x128 element screen with the balance of the display showing stored data. A frame rate of 500 Hz could be achieved.
- picking off a 128x128 element portion of a 244x190 array at the expense of reduced LED duty cycle and brightness (approx. 35%) while maintaining a 240 Hz frame rate.
- Having the CCD array manufacturer modify the on board 244x190 electronics to scan just a 128x128 section. This approach would offer the desired 128x128 organization and the 500 Hz frame rate. The modification was deemed possible, but beyond the scope of the program.

125 lines/inch VIDEO LED DISPLAY

POSSIBLE SYSTEM ORGANIZATION

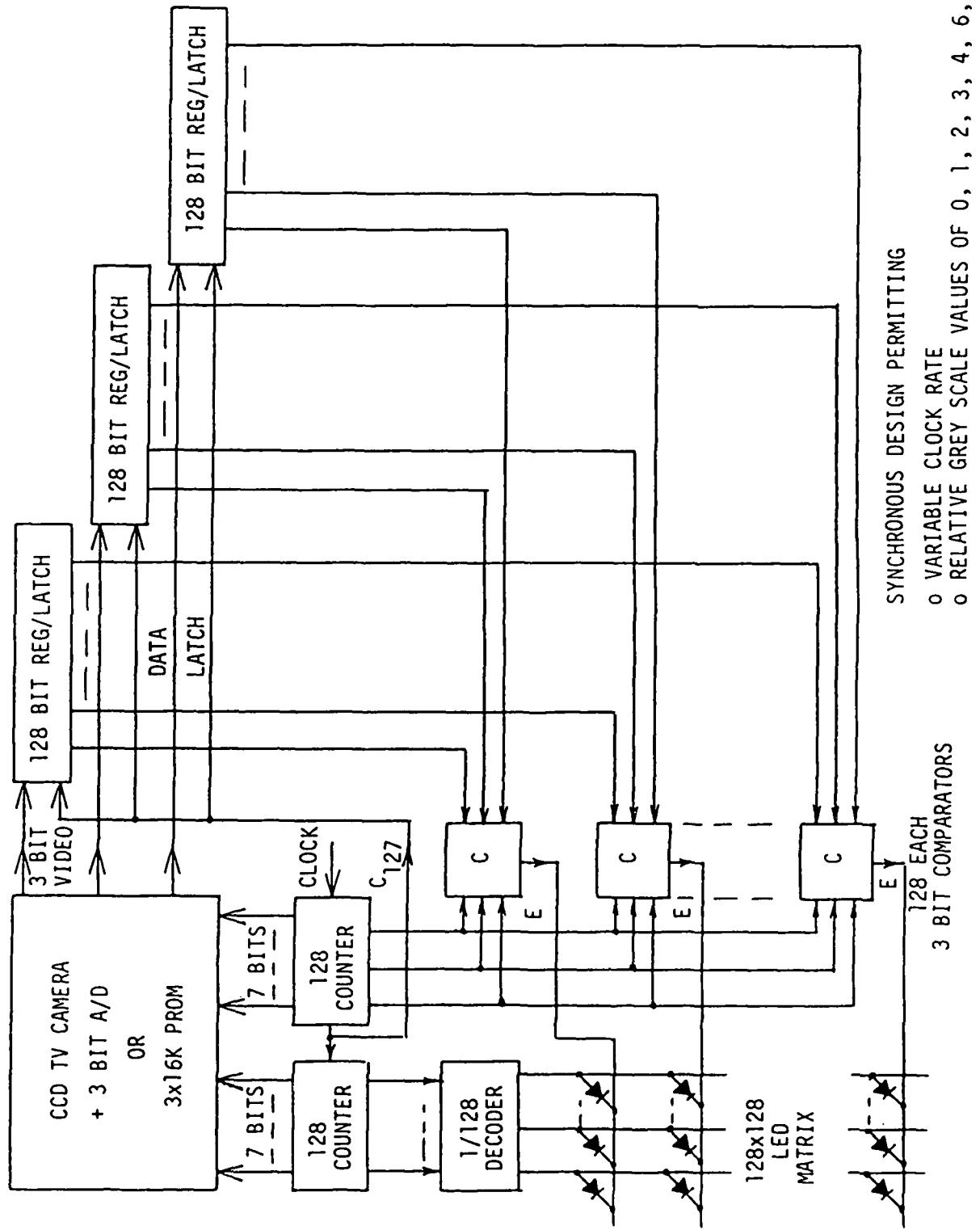


FIG. 19 POSSIBLE SYSTEM ORGANIZATION

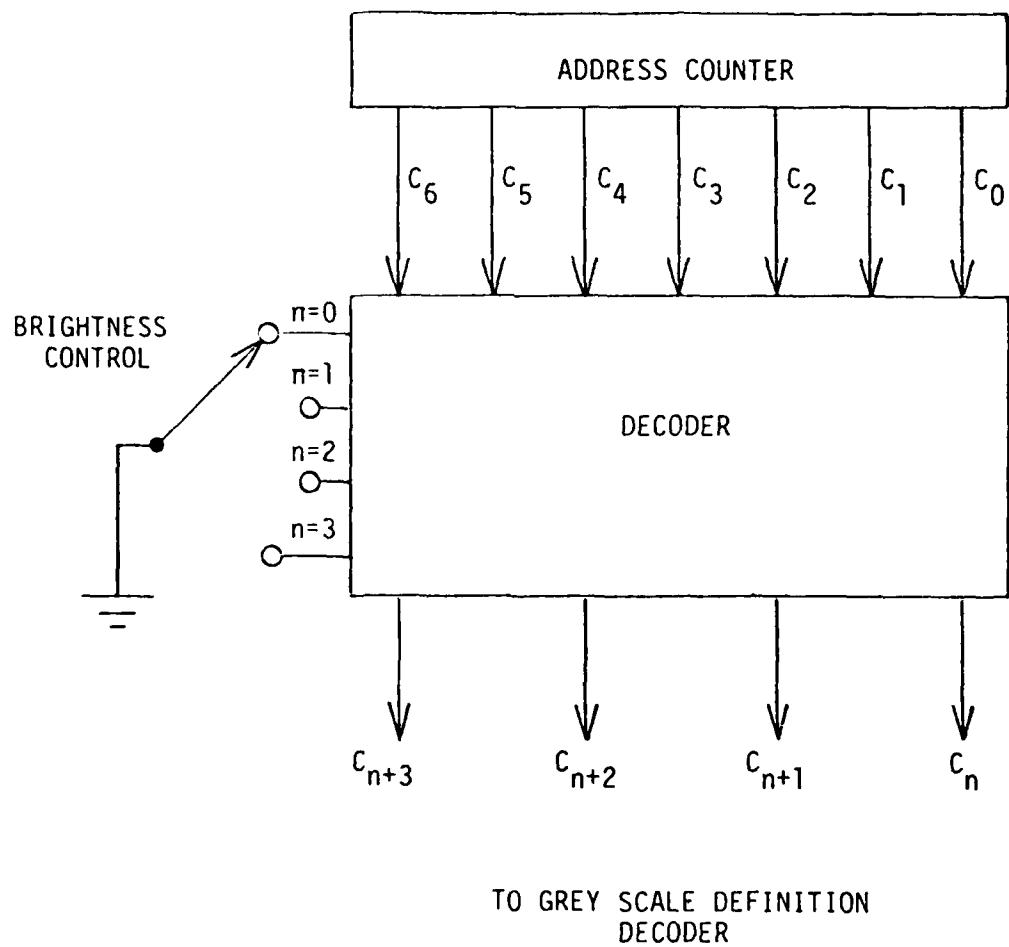
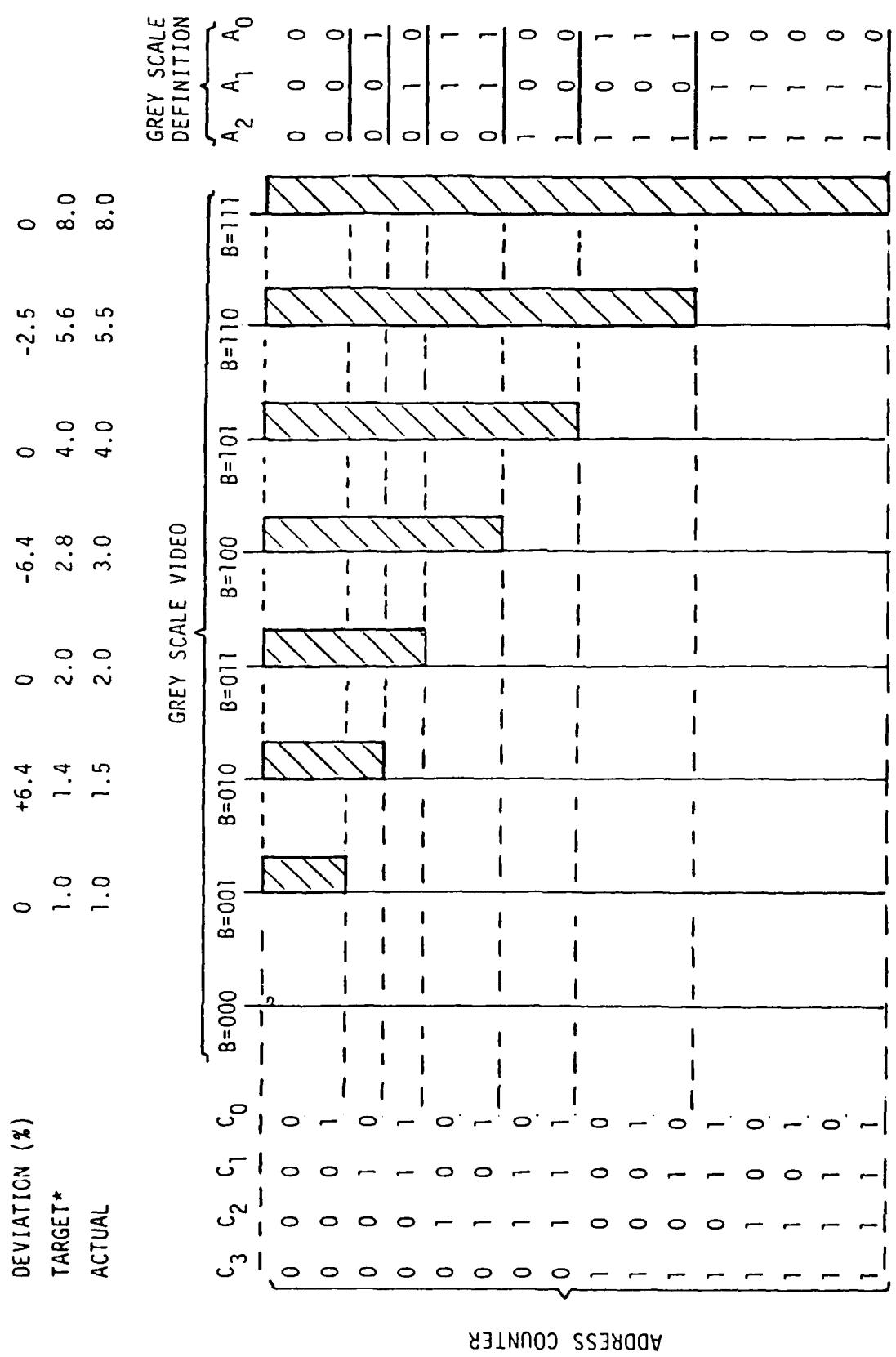


FIG. 18 BRIGHTNESS CONTROL

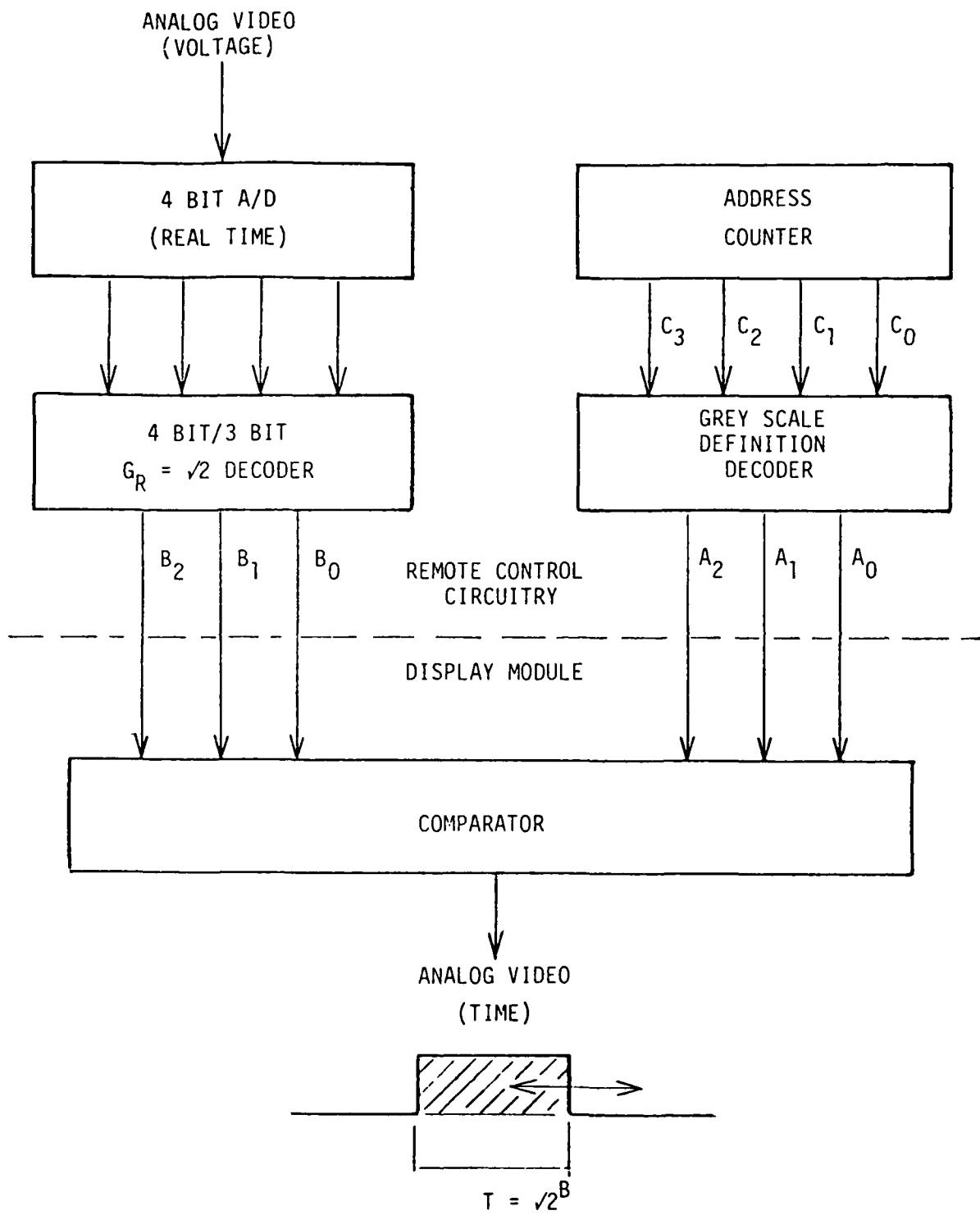
125 LINES/INCH VIDEO LED DISPLAY



\*GREY SCALE RATIO OF  $\sqrt{2} = 1.41 \approx 1.4$

FIG. 17 GREY SCALE RATIO DETERMINATION

125 LINES/INCH VIDEO LED DISPLAY

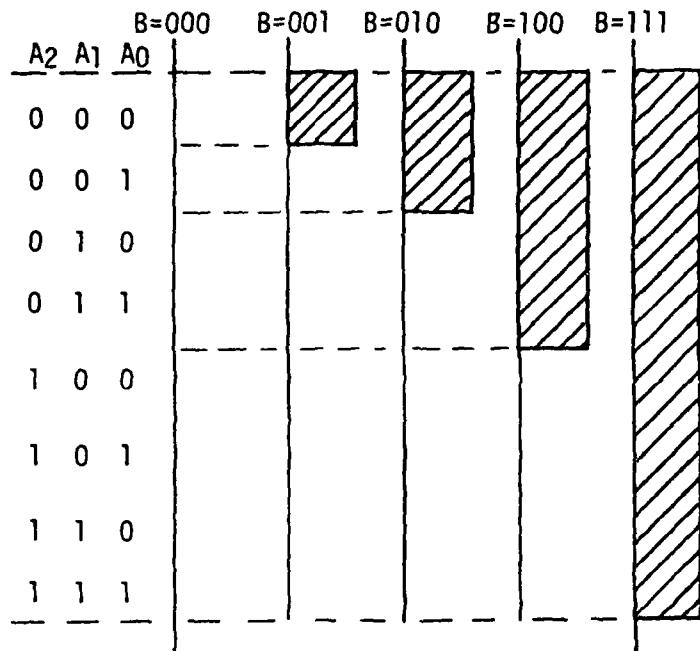


for integer values of  $B$  where  $0 \leq B \leq 6$

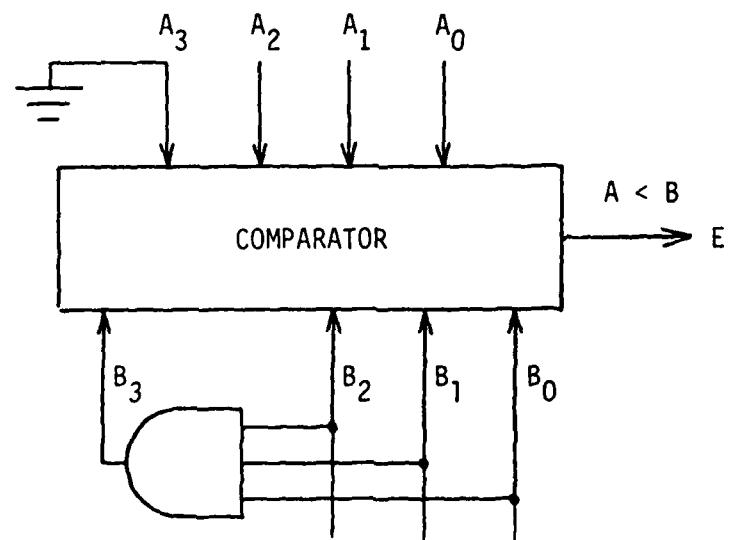
FIG. 16 GREY SCALE IMPLEMENTATION

125 lines/inch VIDEO LED DISPLAY

GREY SCALE



ADDRESS COUNTER



GREY SCALE VIDEO

FIG. 15 VIDEO DISPLAY GREY SCALE

## 125 lines/inch VIDEO LED DISPLAY

### DRIVE CONDITIONS

- o A 128 element linescan with a 1/128 duty cycle is assumed.
- o Extrapolation of column peak current handling capacity based on 64 lines/inch gives  $4.1A \cdot (8/16)^* = 2.05 \text{ AMP}$   
or a peak diode current of

$$2050 \text{ mA} / 128 = 16 \text{ mA}$$

- o The drive condition has therefore tentatively been established as  
16 mA @ 1/128 duty cycle  
with peak column current of 2.05 amps.

- o Assuming that  $V_F$  for 3 mil diodes @ 16 mA is equal to  $V_F$  for 8 mil diodes @ 64 mA,  $V_F$  is taken to be 3.5 volts.
- o Based on the assumed  $V_F$  of 3.5 volts the video display power dissipation at 100% load is

$$2.05A \cdot 3.5V = 7.2 \text{ watts}$$

Corresponding 100% load power dissipation for 64 mA @ 1/64 duty cycle for MMM 64 lines/inch is

$$4.1A \cdot 3.5V = 14.4 \text{ watts @ 100% load}$$

$$14.4 \cdot 0.2 = 2.9 \text{ watts @ 20%}$$

- o Assuming video display power dissipation of 2.9 watts would allow the display to operate  $2.9/7.2 = 40\%$  load with a temperature rise equivalent to that experienced on 64 lines/inch displays.
- o Hopefully the average grey scale distribution should allow operation of the video display without restrictions on display loading.

\* Approximate column width ratio

TABLE 8 VIDEO LED DISPLAY DRIVE CONDITIONS

125 lines/inch VIDEO LED DISPLAY

POSSIBLE SYSTEM ORGANIZATION

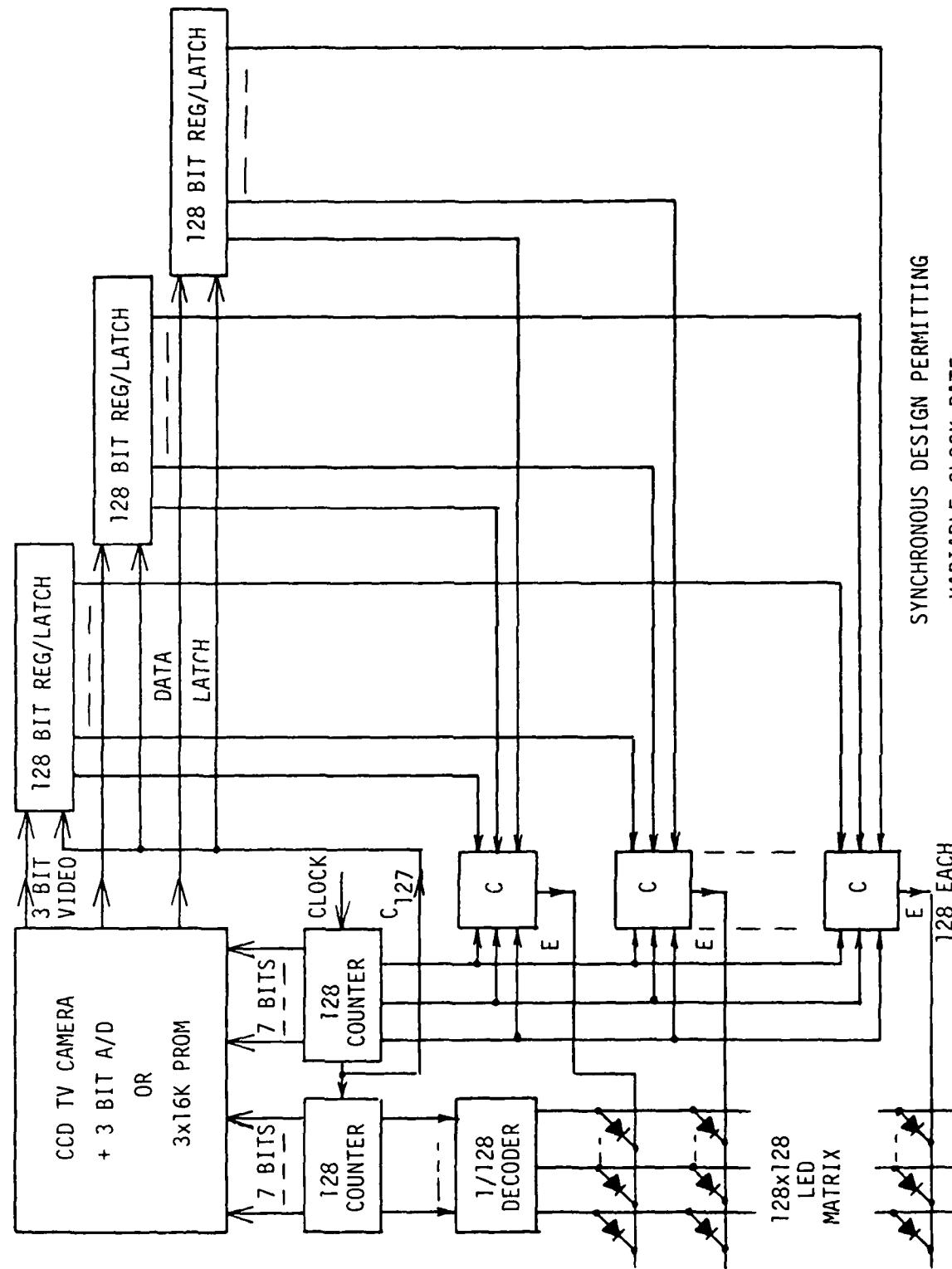


FIG. 14 ELECTRONIC SYSTEM ORGANIZATION

Run 409 SFC Mesa Video Grn.

Probing Results (10 sample die/wafer)

Wafer #100

	-1B	2A	-7	-8, 1A	4D
Thickness (sq. in.)	6.5 - 7	7 - 7.5	7.5 - 8.5	7.5 - 8	7.5 - 8
AN+Top Mesa Dia. (mils)	1.53	3.38	1.65	3.5	1.53
Junct. Bot. Mesa Dia. (mils)		5.1	5.15	4.92	5.03
Epi. Junction Width (mils)		5.07	5.03	4.84	5.03
EL pk	5580				4.96
EL DOM	5628				
$I_c = (\mu W/sr)^*$					
PLIP Probe $I_v$ 10 ( $\mu$ cd)	1651	$\pm 426$	2071	$\pm 297$	1990
$V_F$ 10 (volts)				$\pm 702$	1910
Std. Probe $I_v$ 10 ( $\mu$ cd)	1620	$\pm 837$	1641	$\pm 870$	1689
$V_F$ 10 (volts)				$\pm 540$	$\pm 540$
$V_F$ 20 (volts)	2.24	$\pm .27$	2.22	$\pm .06$	2.26
$V_F$ 20 (volts)	2.46	$\pm .21$	2.47	$\pm .12$	2.58
$V_R$ 100 A (-V)	8/>100		>100		30/>100
$I_L$ 1.1/1.4V ( $\mu$ A)	.02/20		.01/.05		.02/14
$R_d$ 10/20 ( $\Omega$ )	22		25		32
					23
					39

Notes  
 $*I_c = \frac{I_v}{683V_A}$

TABLE 9 SFC MATERIAL WAFER PROBE RESULTS

The experience gained to date has provided insight into the limitations of the present assembly technique.

Pre-bond testing of the assembled array commenced showed that, although the number of non-operating LED's was well within the specified 1%, there were an excessive number of shorts and leakage paths. This was attributed to the tendency for the epoxy to spread between adjacent devices or flow up the edges of the flipped mesa, thereby creating potential anode-anode and anode-cathode leakage paths.

Techniques to clear these shorts were developed and implemented. An electrical method proved effective and most shorts were eliminated.

The difficulties experienced which precluded satisfactory completion of the SFC array are enumerated below. These are primarily associated with the fact that epoxy bumping of contacts is unsatisfactory at 128 lines-per-inch resolution.

- Repetitive epoxy curing cycles required for multiple chips.
- Epoxy smearing contributing to leakage during chip-to-chip and mesa aperture-to-rail alignment.
- Reduced size contacts restrict area available for achieving electrical contact and adequate mechanical strength.
- Variation in mesa etching rates results in size variations, adversely affecting electrical contact and mechanical strength.
- Variation in wafer flatness/thickness results in mesa height variations adversely affecting electrical contact and mechanical strength.
- Saw vibration during isolation cutting affects integrity of epoxy bumps.

- Damage created in rework attempts.
- Damage created in efforts to cure leakage.

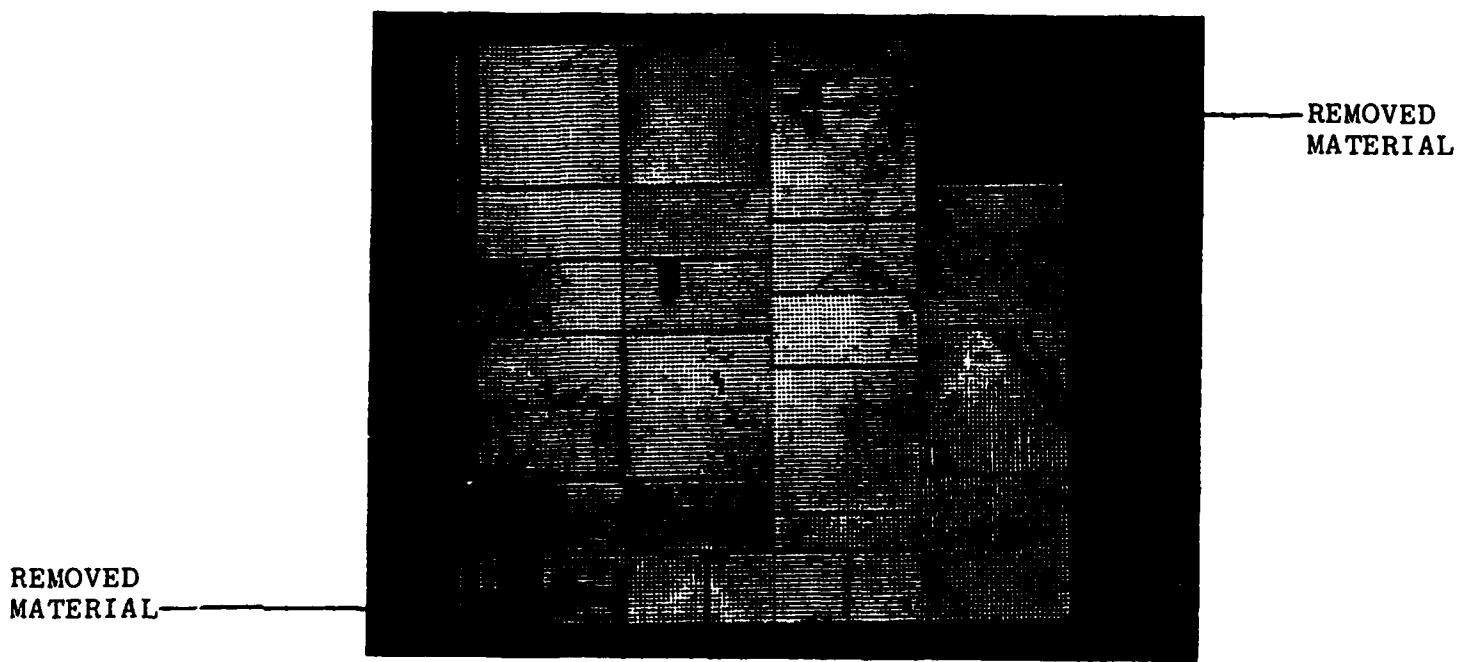
In attempting to overcome these difficulties approximately 55% of the LED array surface was replaced. This extensive rework involved considerable effort. At the point where the DITC/Optotek funding became depleted the approximately 10% of the LED array material which had been damaged during previous repair attempts had been removed. Fig. 24 is a photograph of the array showing the rework sections.

(A superficial contradiction exists between this situation and the relative ease with which the 18x32 sample array was assembled; this is attributable to the fact that the sample array involved a significantly smaller area of array and carrier and that multiple chip-to-chip alignments were not required.)

It was estimated that considerable man hours would be needed to complete repair, bond and test the array. The chances were high that additional damage would be induced during the completion attempts: the prognosis for success was only 50%. This situation, in combination with funding expiry, resulted in termination of effort.

Feb 83

125 LINES/INCH VIDEO RESOLUTION DISPLAY



Present 128x128 element SFC  
array status

FIG. 24 REWORKED SFC ARRAY

#### 4.0 PUBLICATIONS

Optotek presented a paper on the video project at the NAECON conference held in Dayton in May, 1982. This paper essentially summated the technical achievement of the program and included information on system implementation and on the anticipated performance of improved video arrays.

## 5.0 CONCLUSION

The USAF/DITC statement-of-work identified the achievement of a display incorporating the following features:

1. 128 line-per-inch resolution
2. sunlight-readable performance
3. 4-edge abutability
4. full flip-chip construction
5. high speed video imagery
6. contrast ratio of 4:1 in 10,000 ft-candle ambient,  
and, via expansion of program scope,
7. eight grey shades (four in SOW)
8. module-compatible electronics organization

Objectives (1), (7) & (8) have been realized in a 1"x1" demonstration display configuration.

A partial, 18x32 element, semi flip-chip array was built to demonstrate the achievement of performance levels necessary for sunlight visibility.

Attempts to complete a 1"x1" semi flip-chip array were unsuccessful; the primary contributory factor was the difficulty in achieving successful epoxy bump bonding at 128 lines per inch over full-size modules.<sup>†</sup> It is felt that this problem could be alleviated to a large degree if further development work was conducted on epoxy bumping techniques and alternate solder-bumping procedures. It is also felt that the SFC procedure could be applied with greater success to lower resolution video arrays - 100 lines-per-inch or thereabouts.

<sup>†</sup> Epoxy bumping had previously been done successfully for 1"x1" arrays but at 64 lines-per-inch resolution.

Since a fully useable array was not available no effort was expended on detailed evaluations of display legibility; however, basic measurements of display light output confirmed that the statement-of-work contrast ratio objectives should be realisable in an semi flip-chip configuration.

The camera used with the demonstration electronics was not compatible with the high speed video imagery requirement of the statement-of-work. Cameras which operate at higher (500 Hz) are now available and the USAF is understood to be considering replacing the GE camera supplied with the system. This will significantly enhance display demonstrations.

Consistent with the R&D nature of the contract, effort was applied to building an array demonstrating abutability in a full flip-chip (FFC) configurations - (3) and (4) above. This was not successful due primarily to material limitations encountered; in addition it must be recognized that it is difficult to build FFC's using higher performance LPE material.

The options which, at contract completion, were deemed to exist for further constructive work leading towards the manufacture of video resolution display modules are outlined below.

In all cases it is recommended that resolution specifications should be modified from 125 lines-per-inch to a lower, but still highly viable, resolution of the order of 100 lines-per-inch. It would still be feasible, for electronics convenience, to fabricate the arrays as 128x128 element modules; for 100 line-per-inch resolution this would expand module size from 1.024" to 1.28". Alternatively, consideration could be given to establishing a module size based on 64x64 elements (0.64"). Array construction would be considerably facilitated by this reduction in size but the space available for location and interconnection of integrated drive electronic circuitry becomes restricted, necessitating detailed trade-off analysis.

## Monolithic Standard Stitch Bond (SSB) Construction

### Advantages

- Sunlight visible performance achievable
- Fabrication feasible without further development
- Relevant to immediate markets.
- Two-edge abutability feasible for 125 line-per-inch; four-edge abutability potentially feasible at 100 lines-per-inch.

### Disadvantages

- Performance is inferior to semi-flip chip in same material
- Four-edge abutability not feasible at 125 lines-per-inch.

## Monolithic Semi Flip-Chip (SFC) Array

### Advantages

- Optimum performance
- Two-edge abutability feasible; more amenable to four-edge abutability. Also four-edge abutability potentially feasible at 100 lines-per-inch.

### Disadvantages

- Epoxy-bumping not feasible at 125 lines-per-inch, although it is potentially feasible at 100 lines-per-inch. The alternative solder bump technology requires further extensive development in application to LED materials and arrays.

Optotek's recommendation for future would involve the use of SSB or SFC technology to construct an abutable array at 100 lines-per-inch. Details have been presented to both the USAF and DITC; it has been accentuated that it will be necessary to have available a suitable complement of custom integrated circuits in order to construct a fully demonstrable miniaturized display system and to participate in emerging markets for video resolution LED display products.

**END**

**FILMED**

**8-85**

**DTIC**